

Fig. 1

Fig. 2

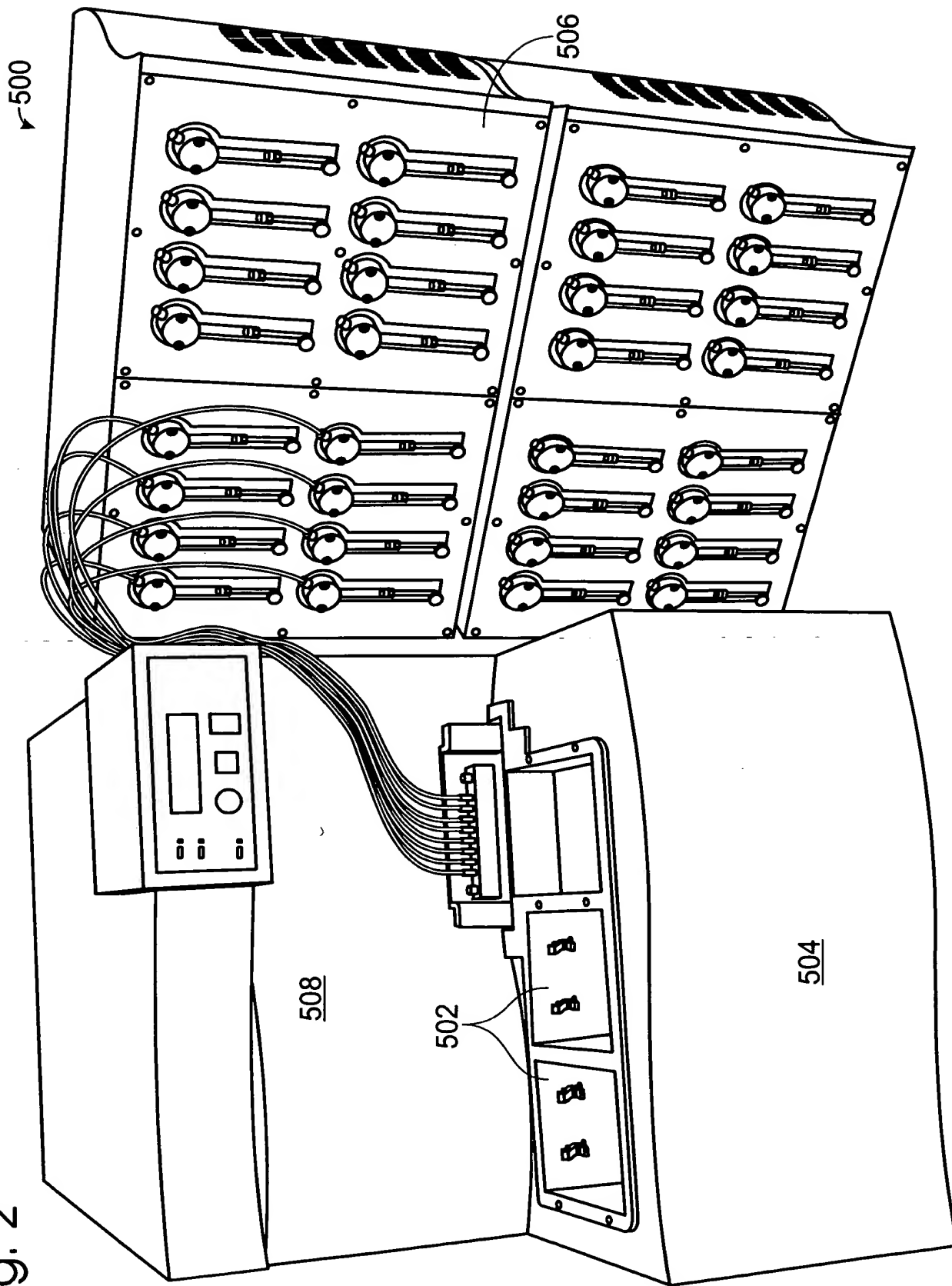


FIG. 2

Fig. 3

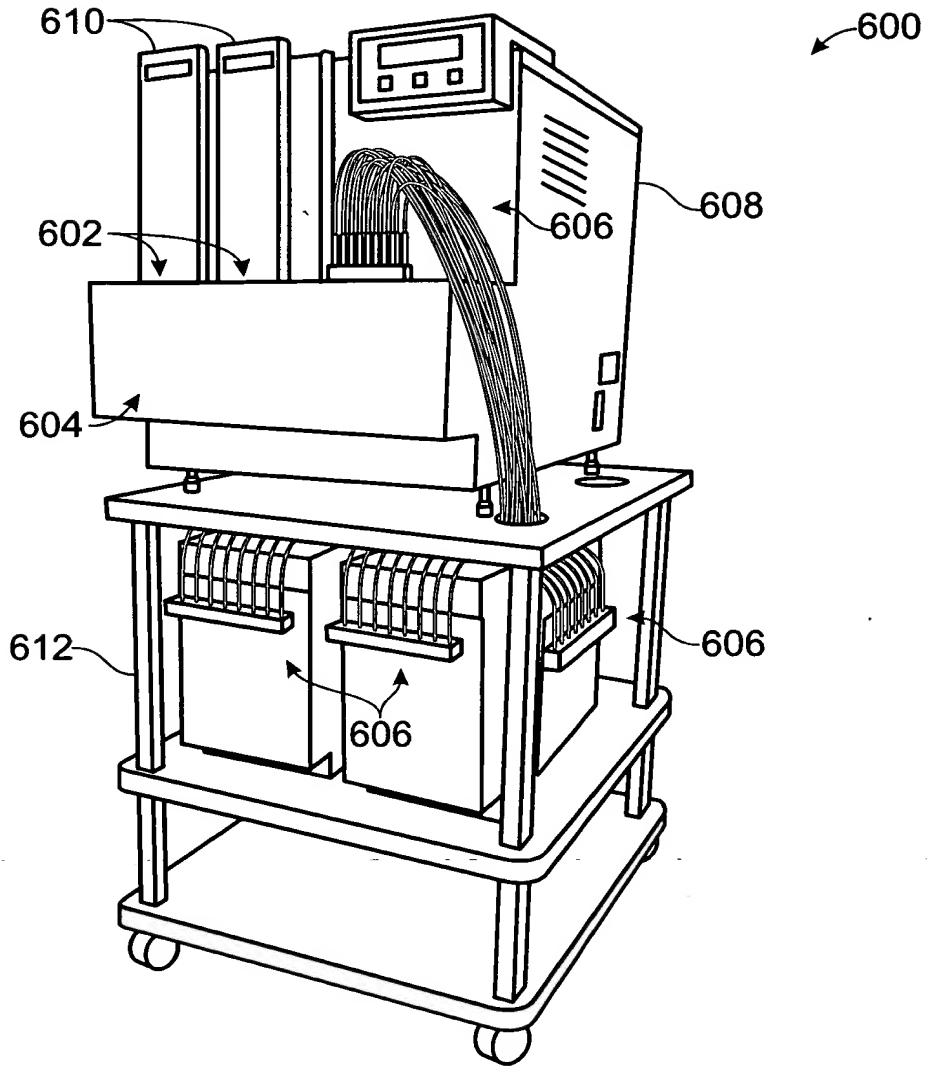
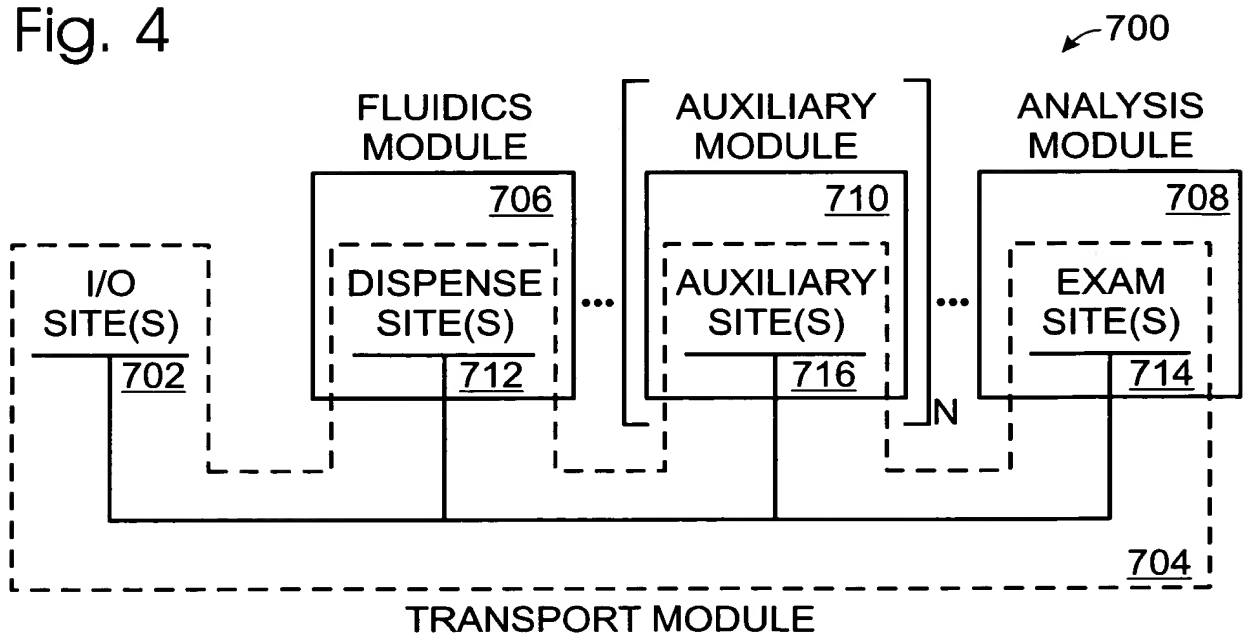


Fig. 4



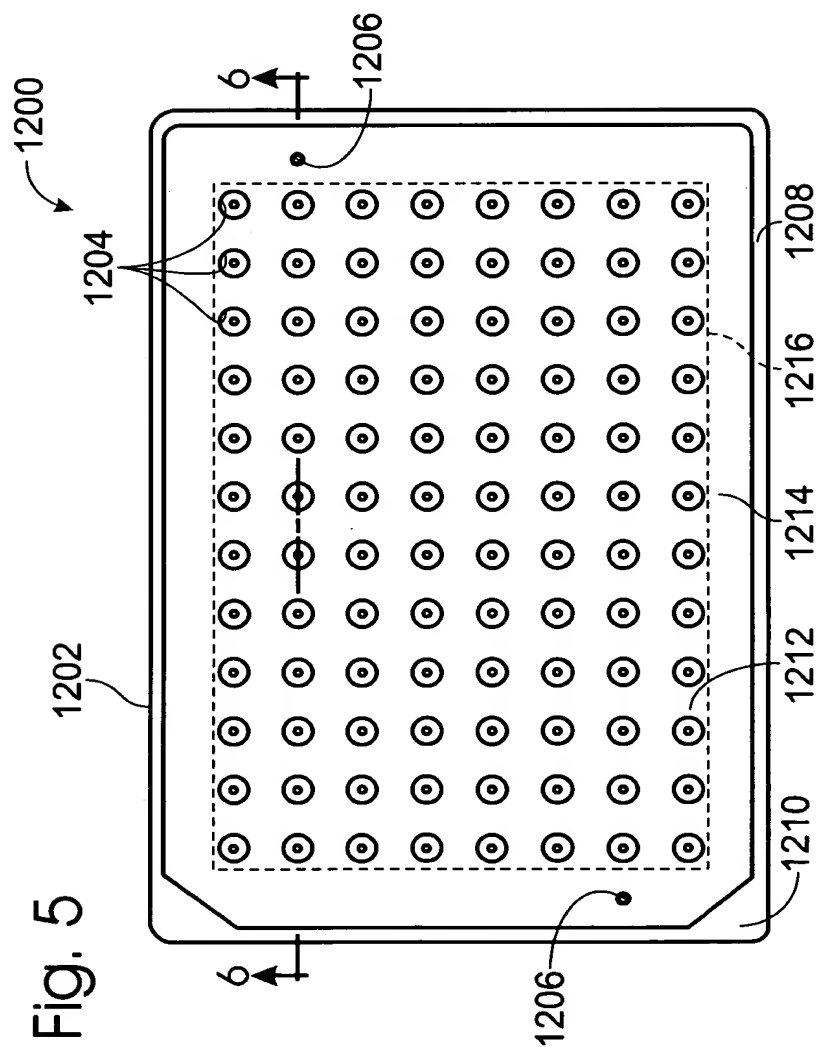


Fig. 5

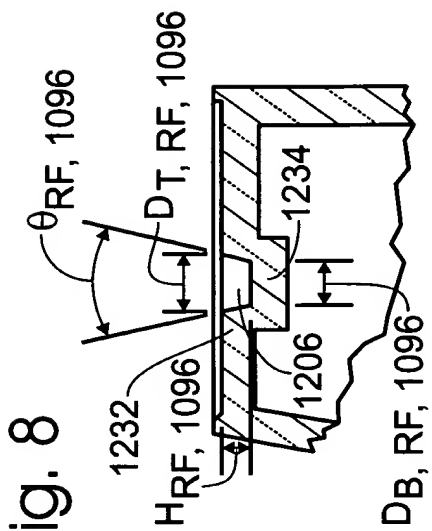


Fig. 8

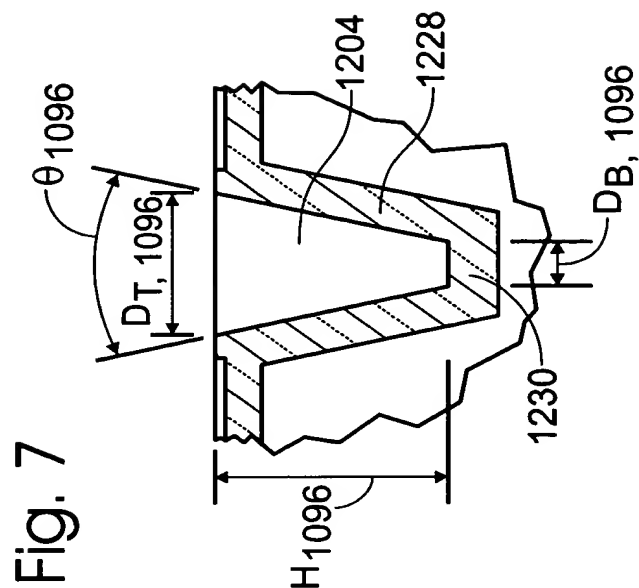


Fig. 7

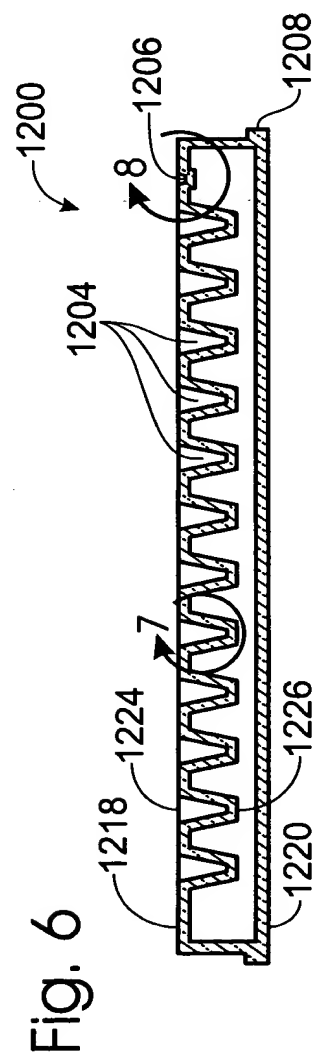


Fig. 6

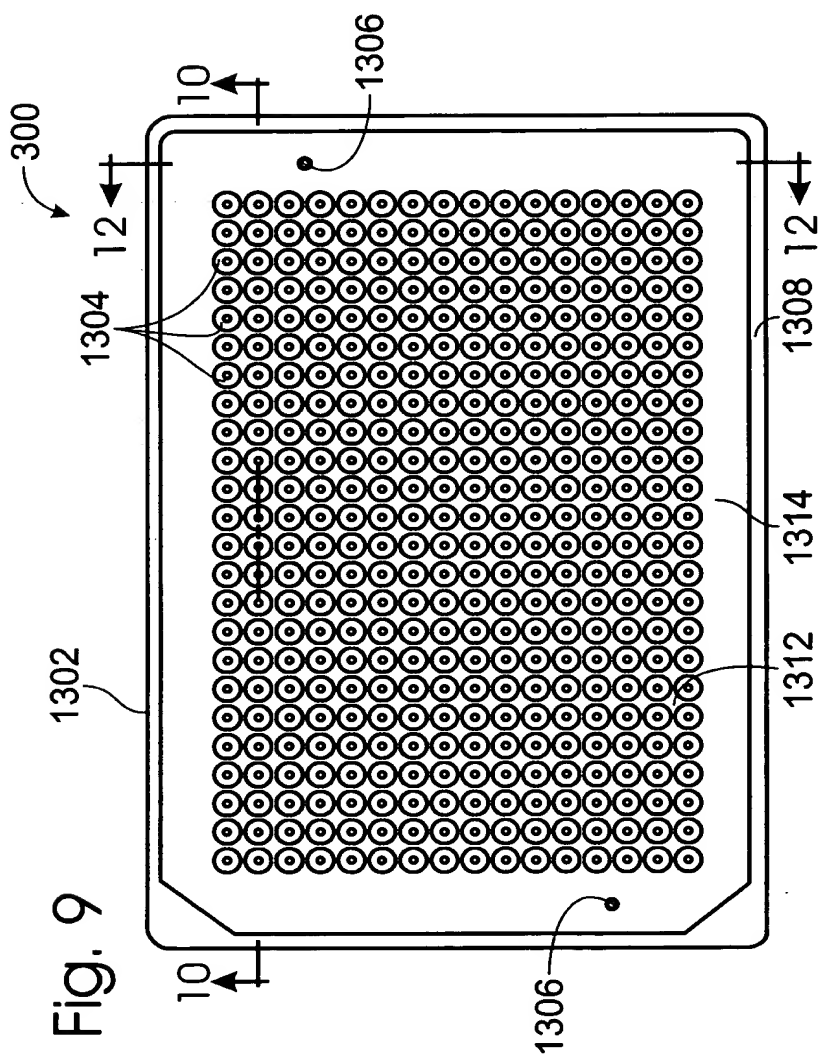


Fig. 12

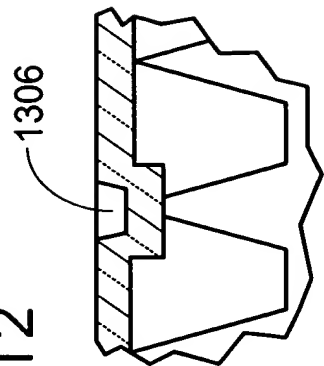


Fig. 11

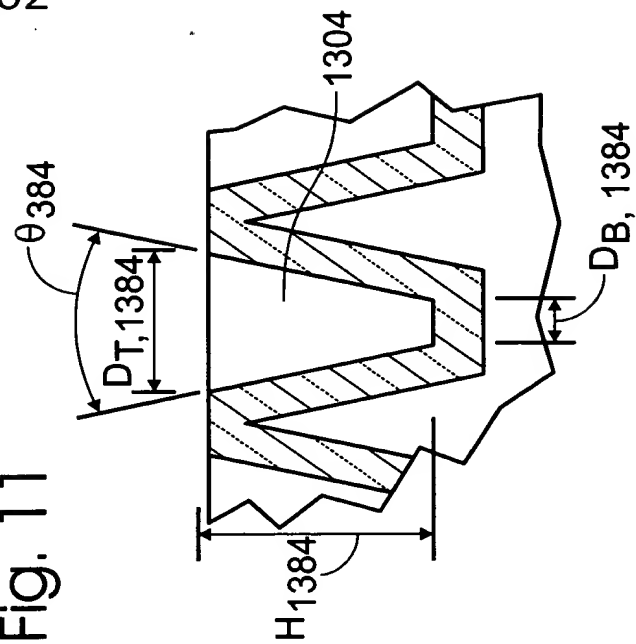


Fig. 10

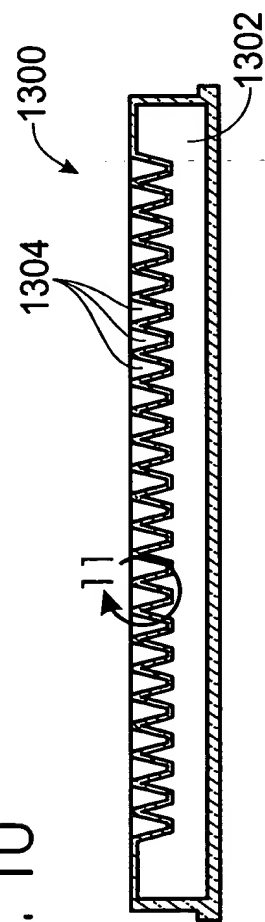


Fig. 13

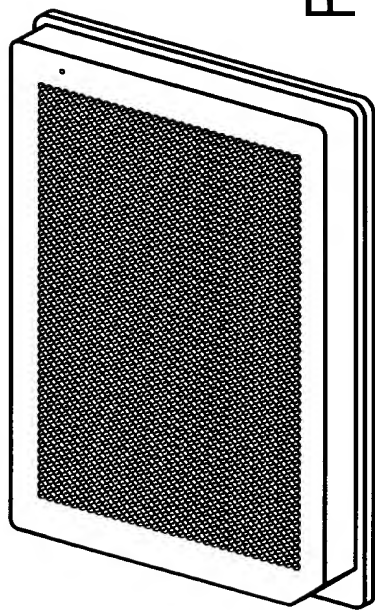


Fig. 15

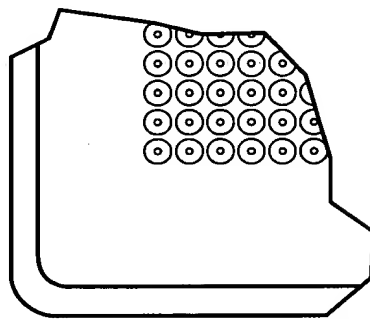


Fig. 17

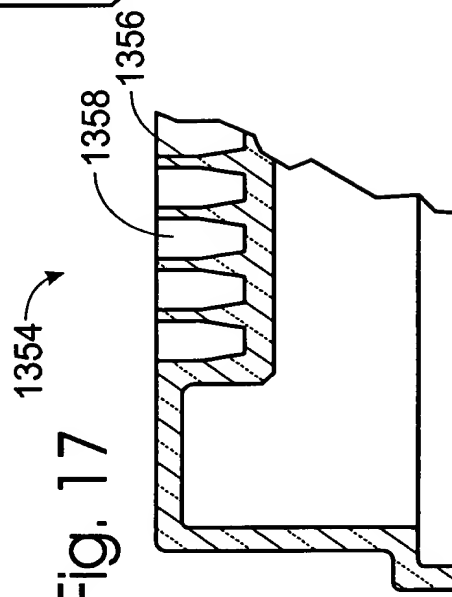


Fig. 16

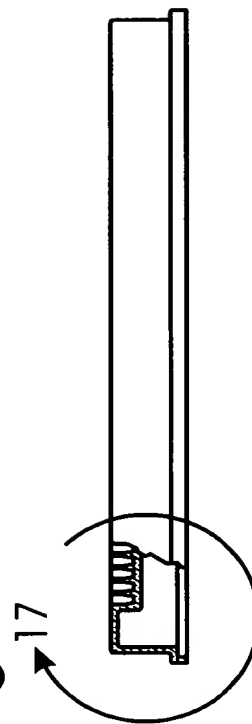
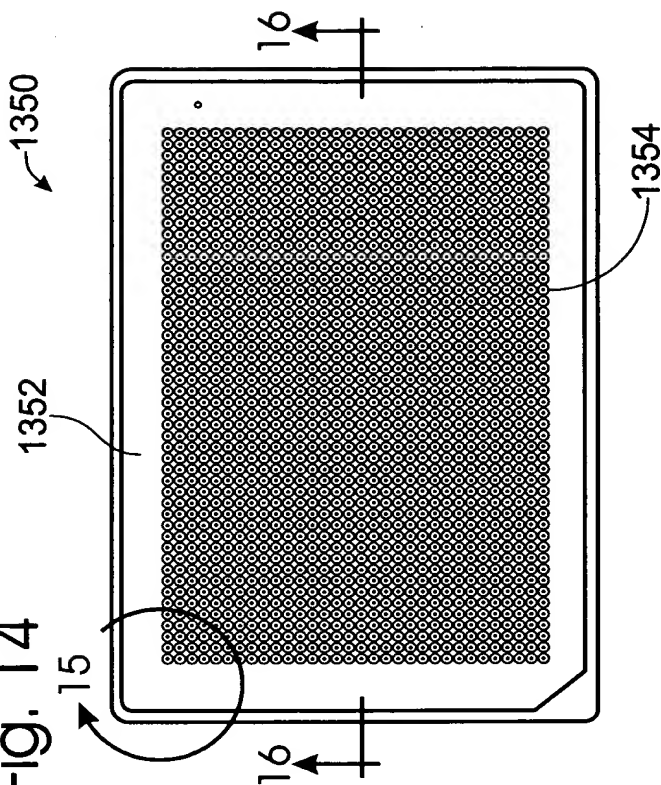


Fig. 14



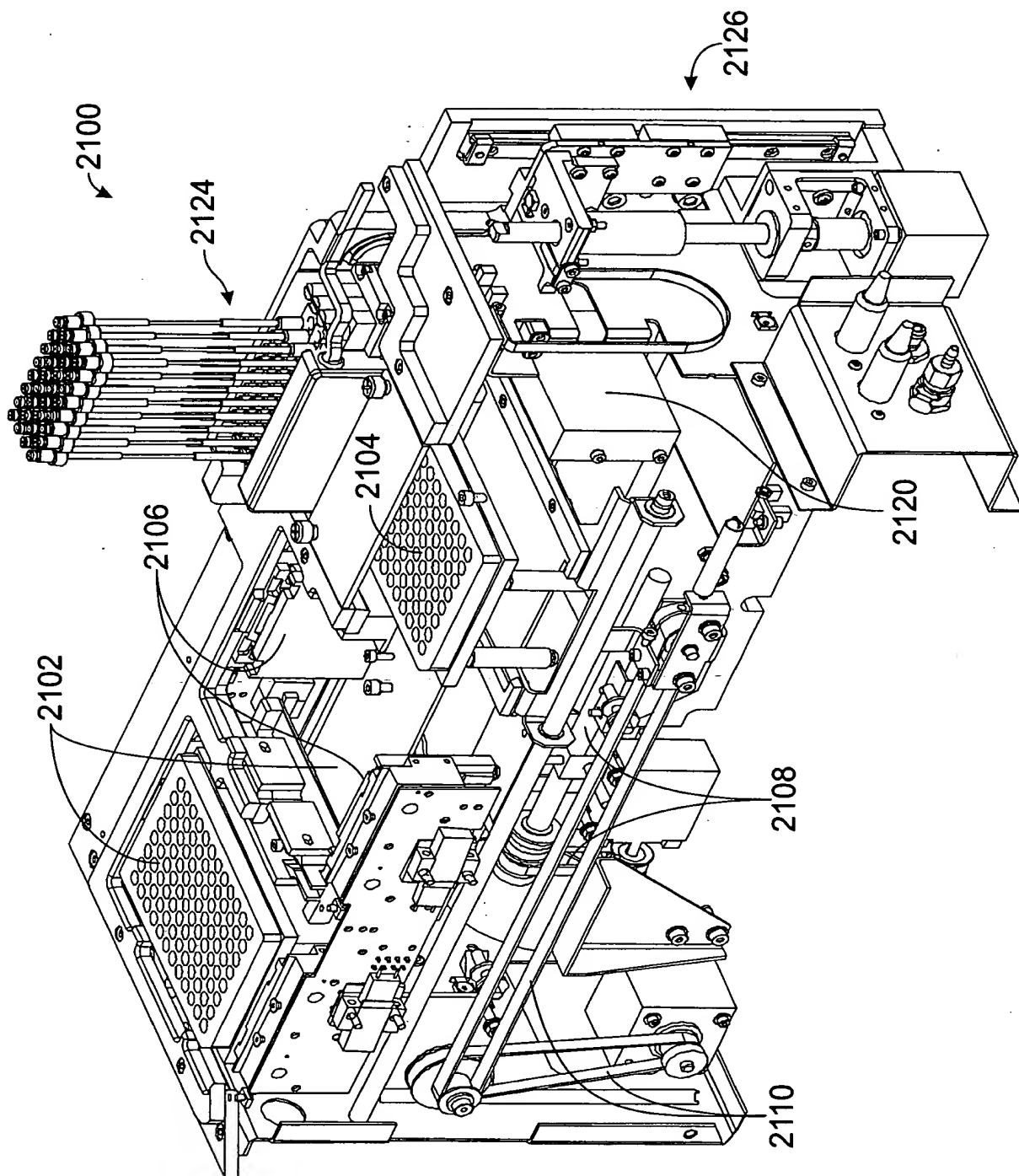


Fig. 18

Fig. 19

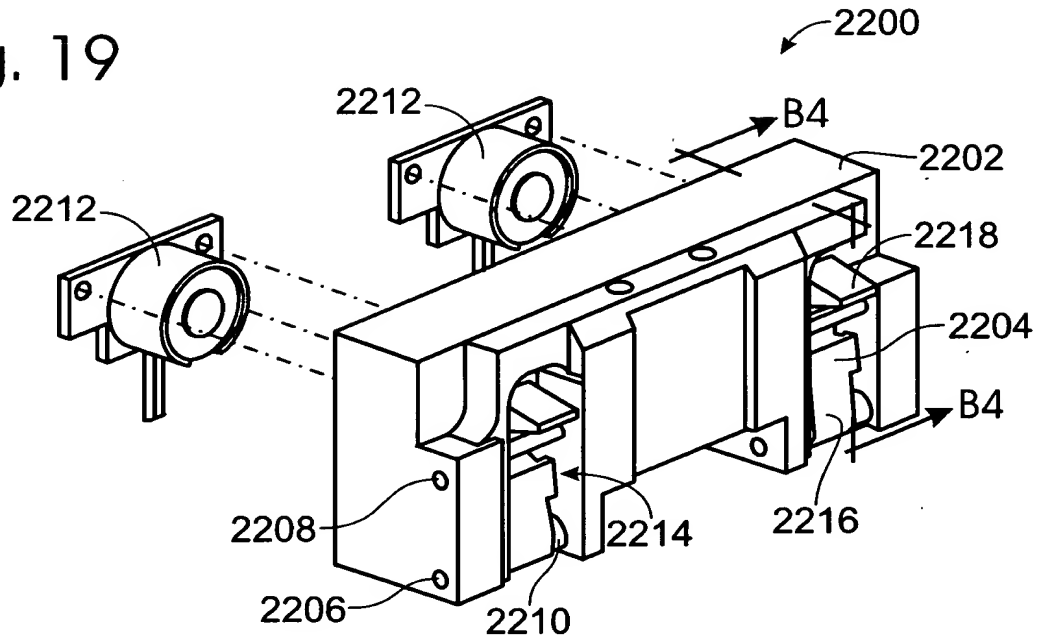


Fig. 20

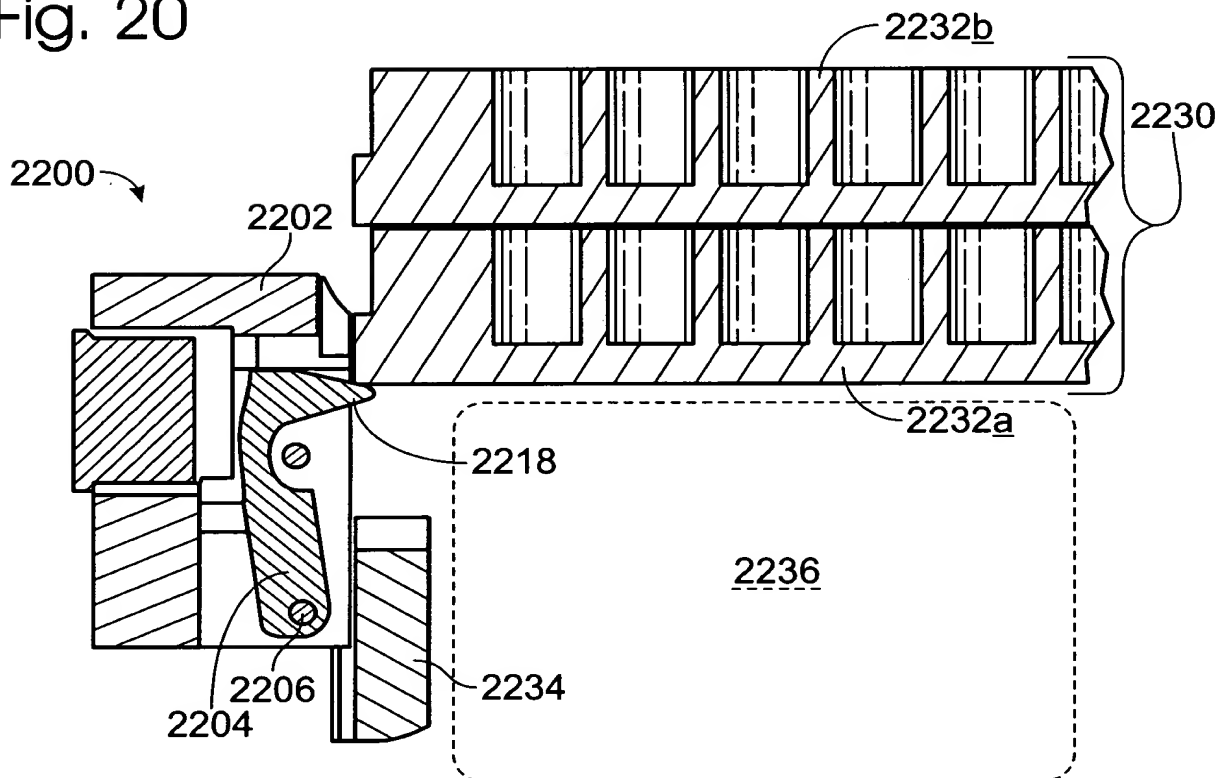




Fig. 21 (INPUT CYCLE)

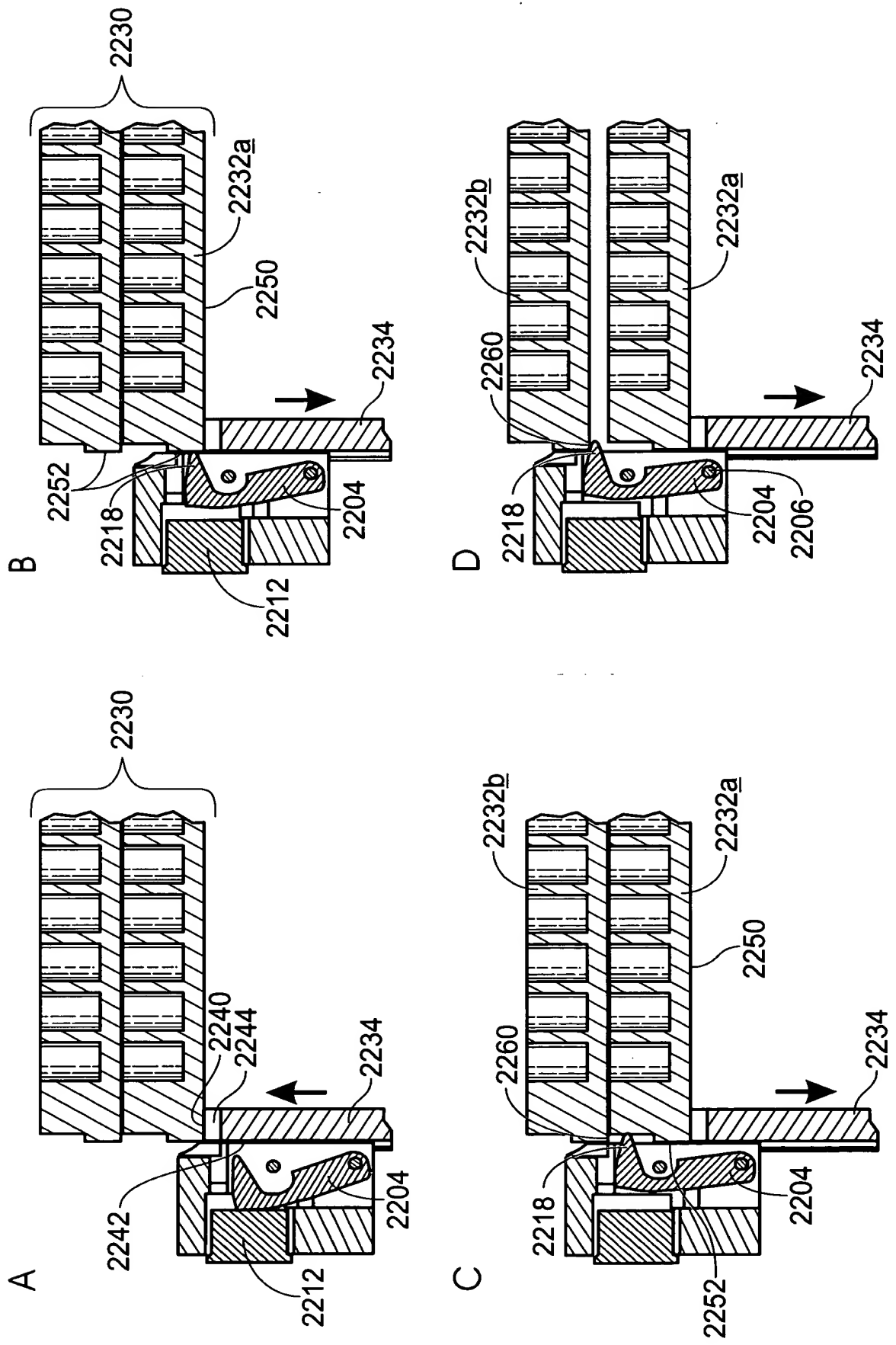


Fig. 22 (OUTPUT CYCLE)

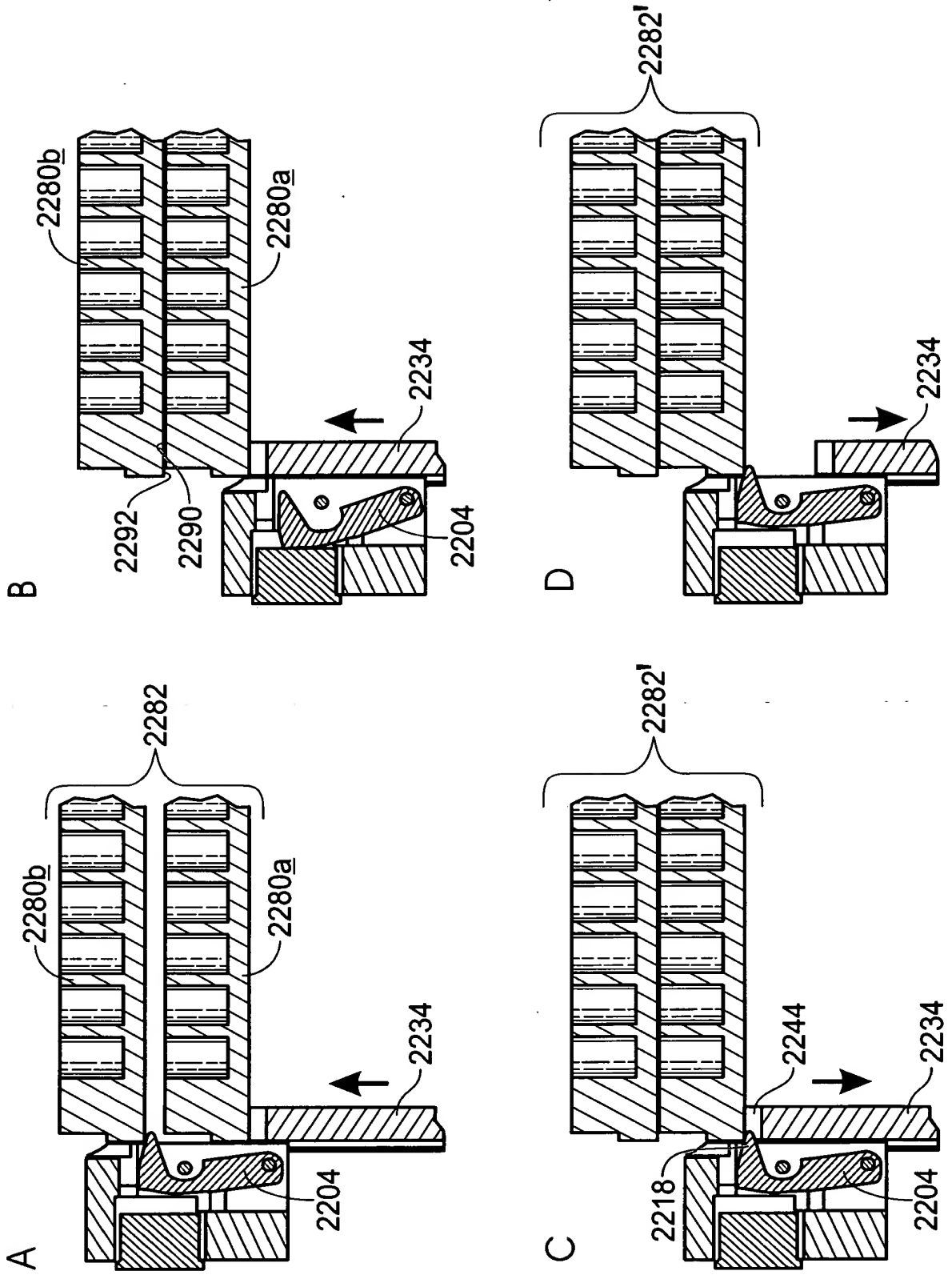


Fig. 23

2300

2310

2308a

2308b

2306

2302

A

2354

2356

2340

2344

2348

B

2342

C

2350

2352

2344

2326

2328

2322

2320

2330

2304



Fig. 25

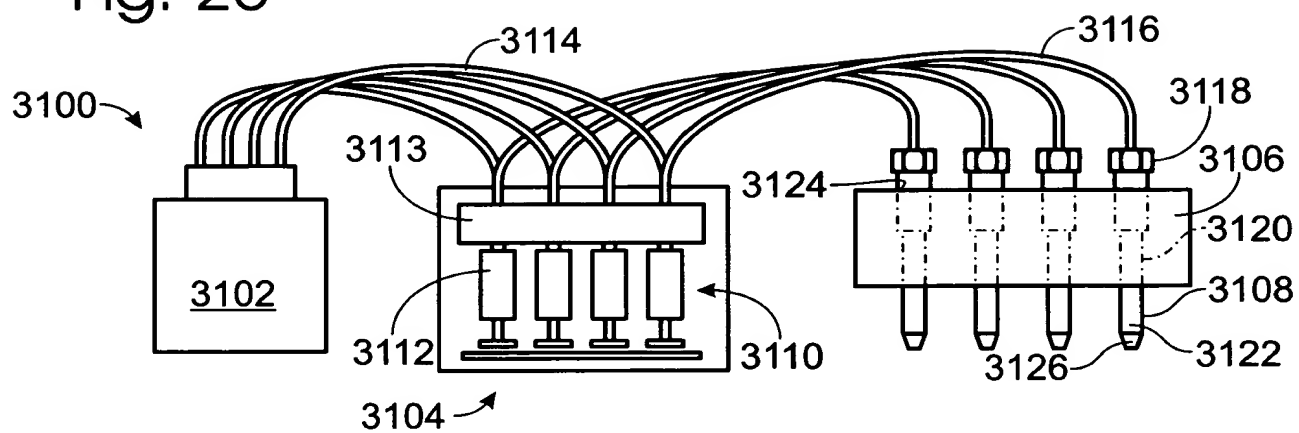


Fig. 26

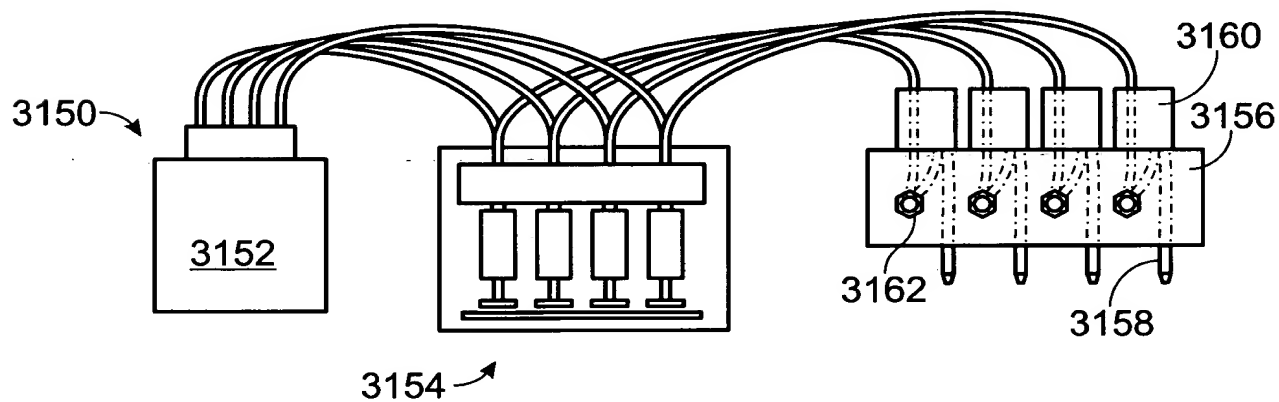


Fig. 27

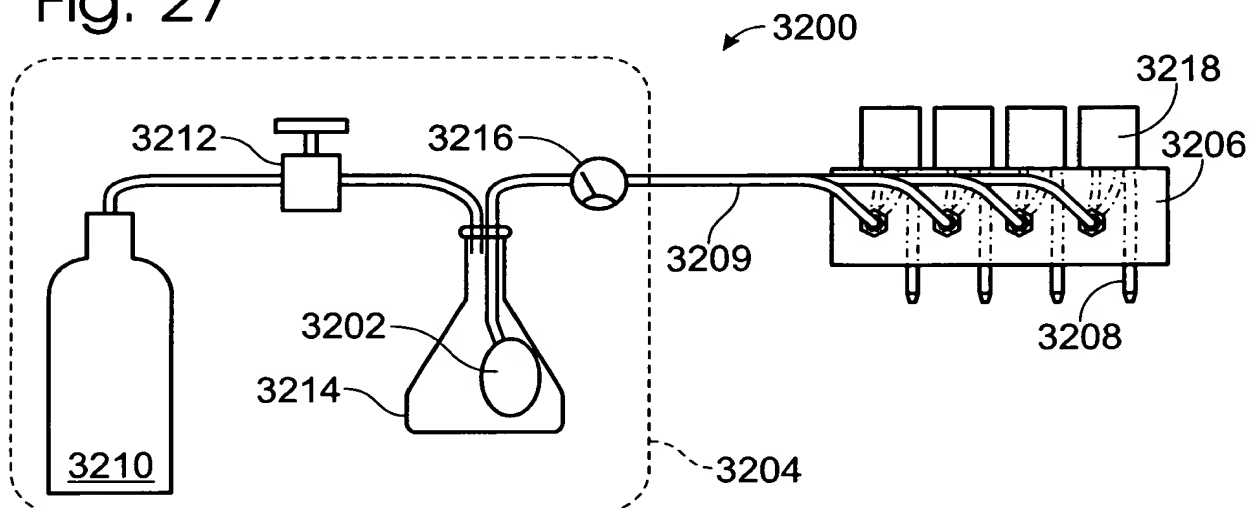
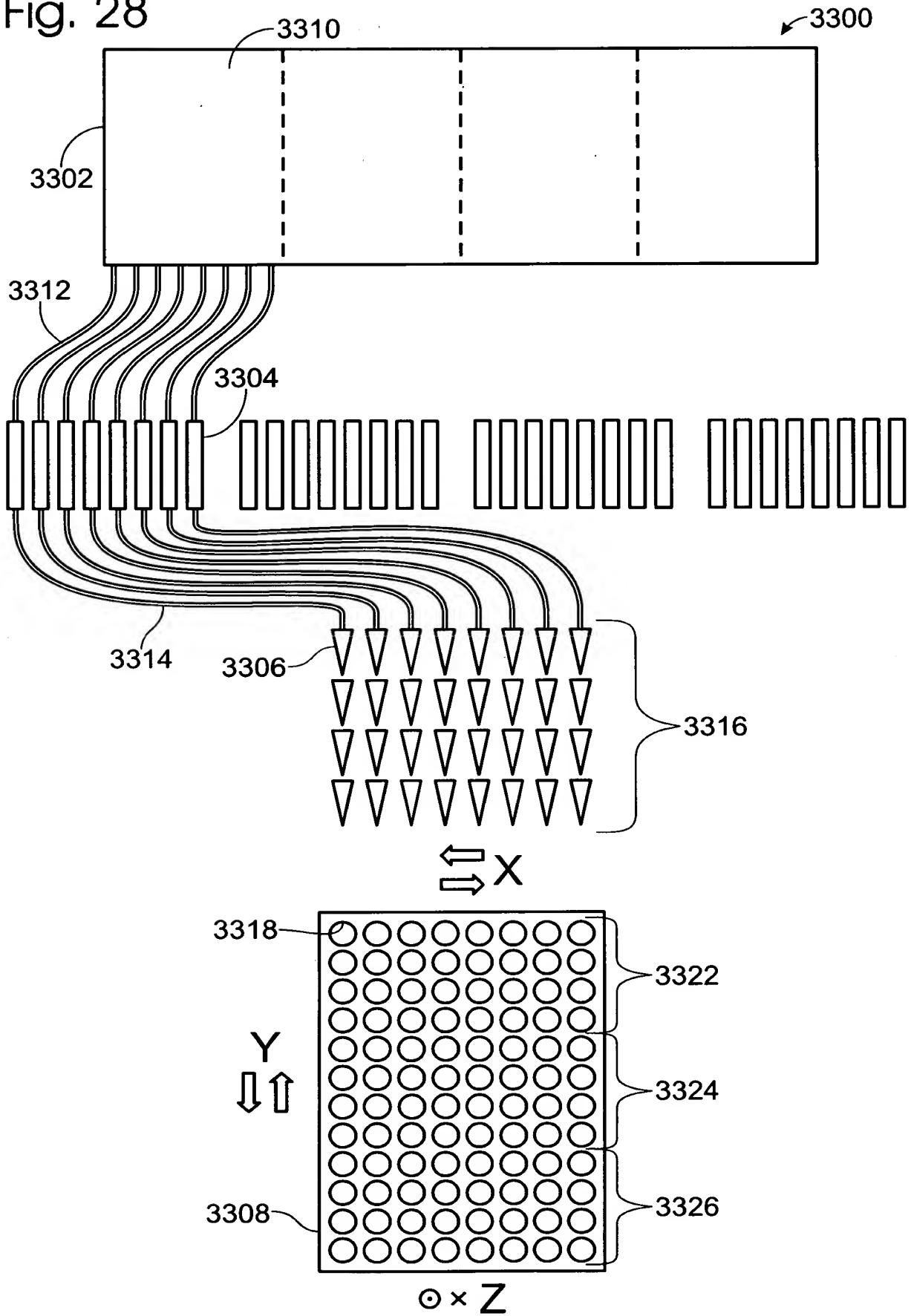


Fig. 28



3410

Fig. 30

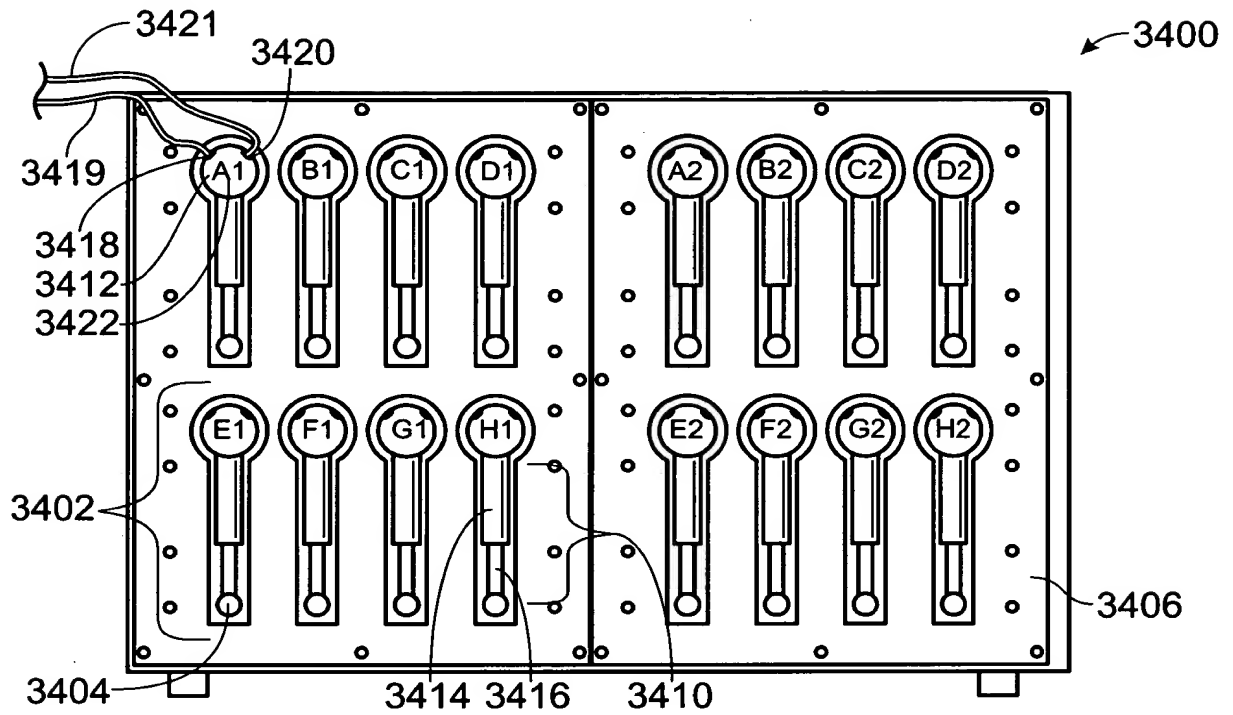
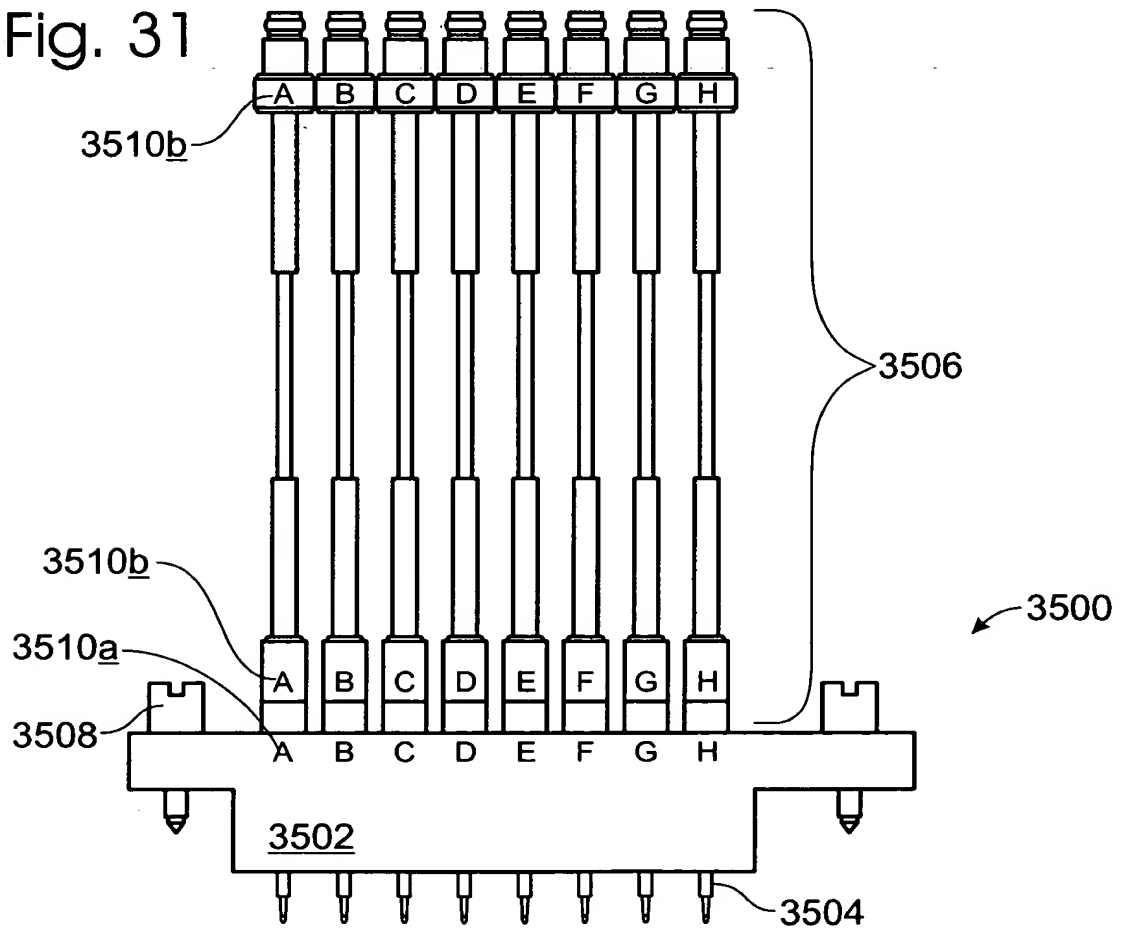


Fig. 31





[illegible]

Fig. 33

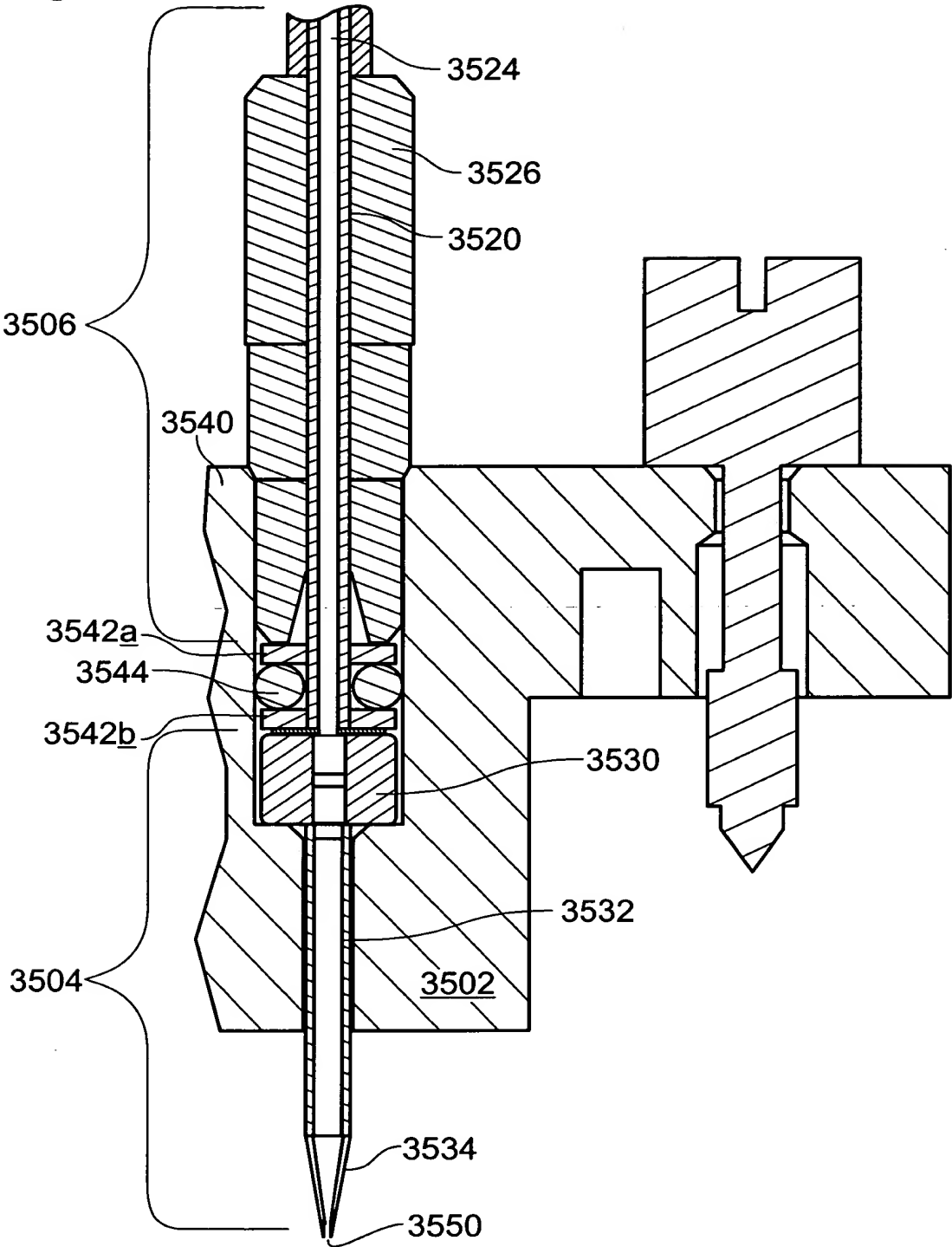


Fig. 34

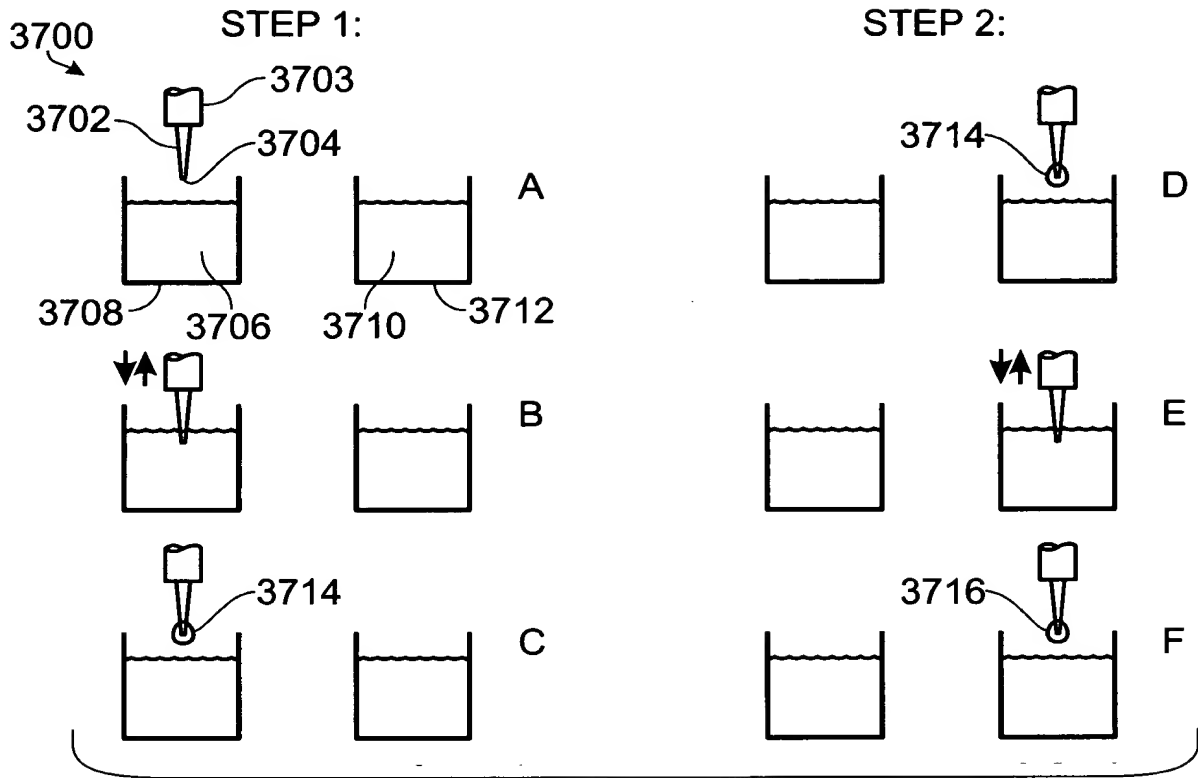


Fig. 35

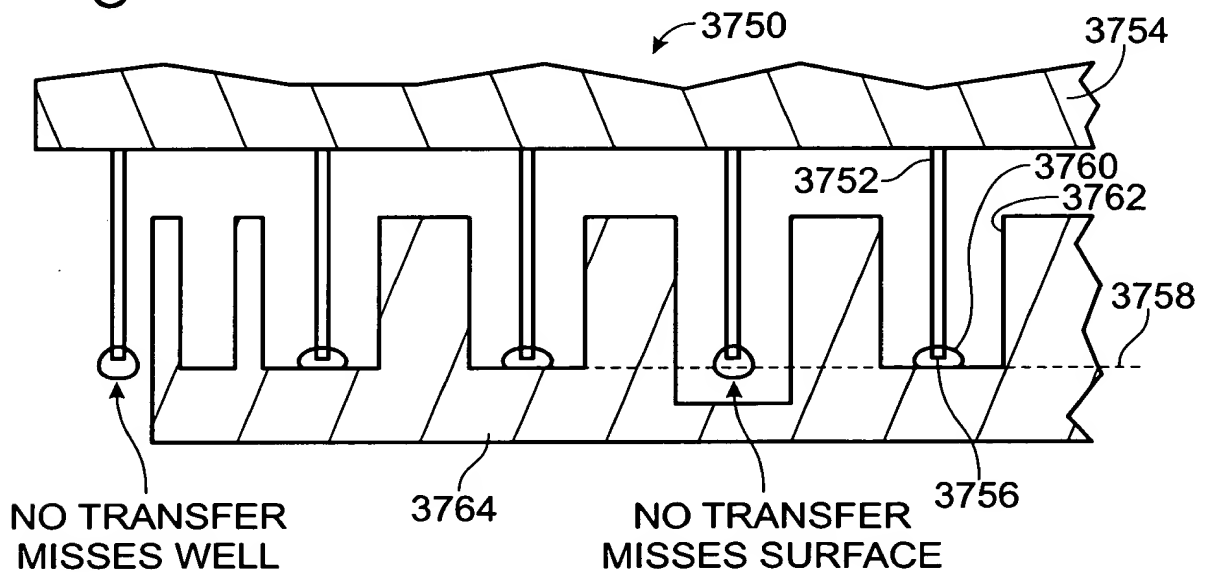


Fig. 36

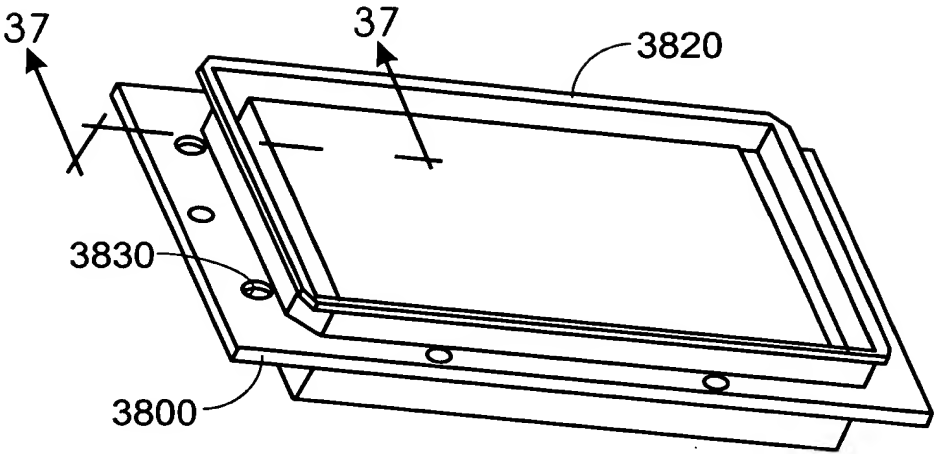


Fig. 37

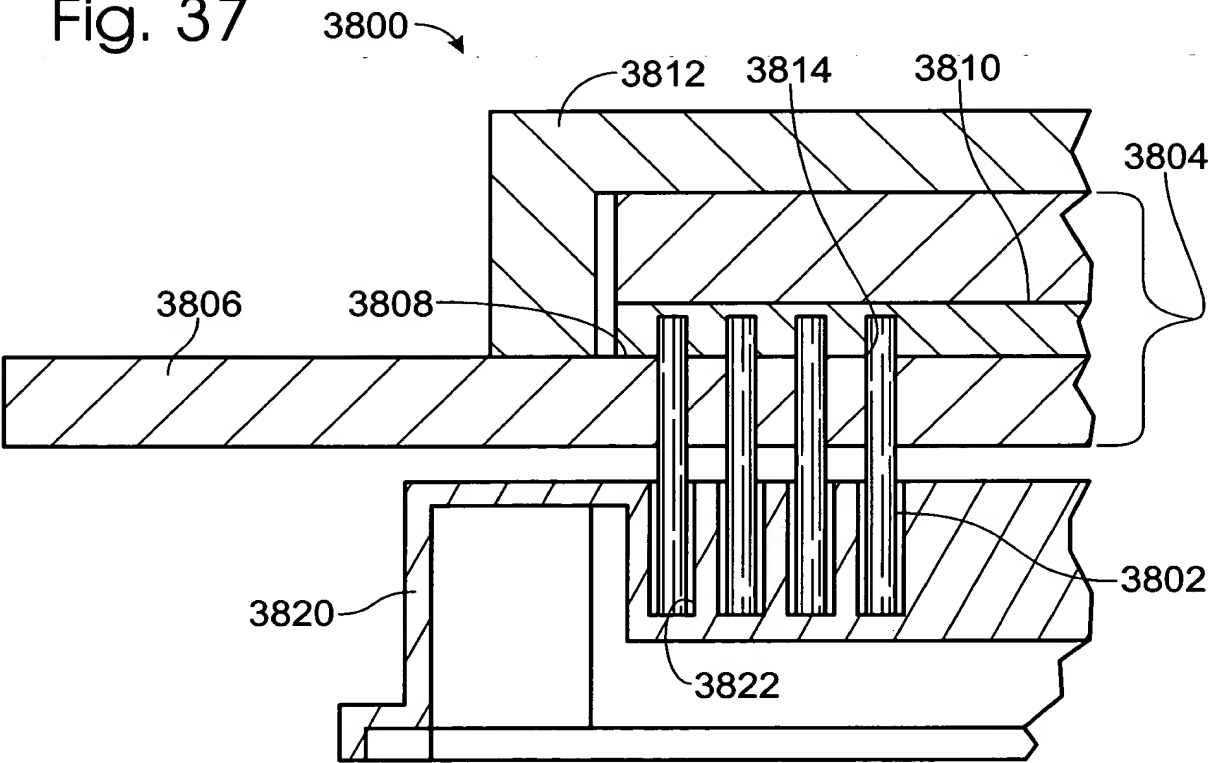


Fig. 38

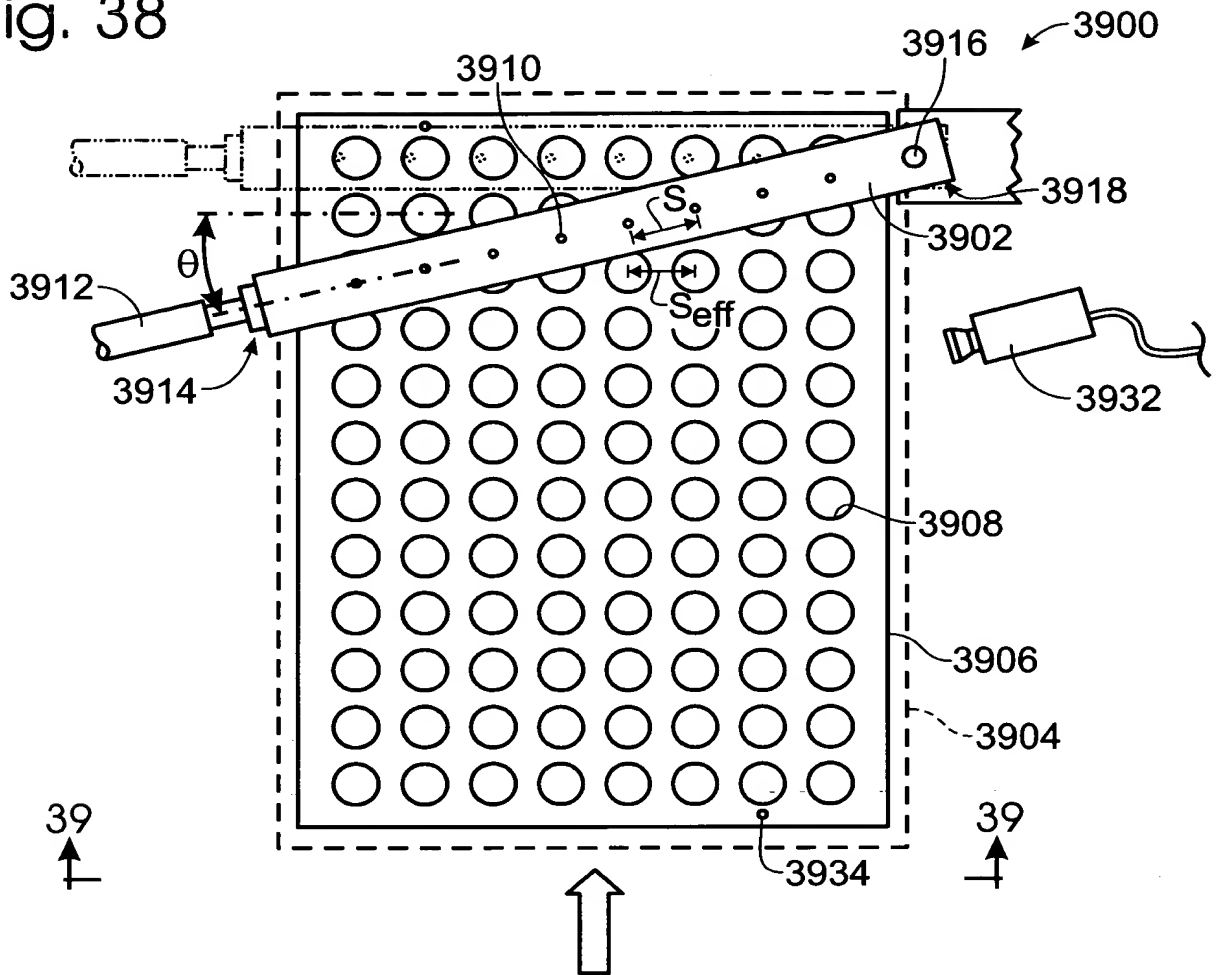


Fig. 39

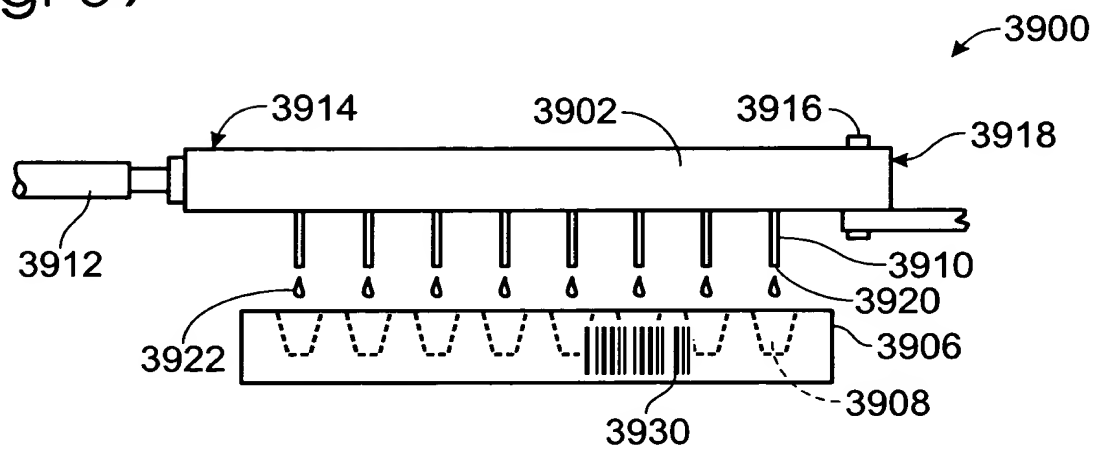


Fig. 40

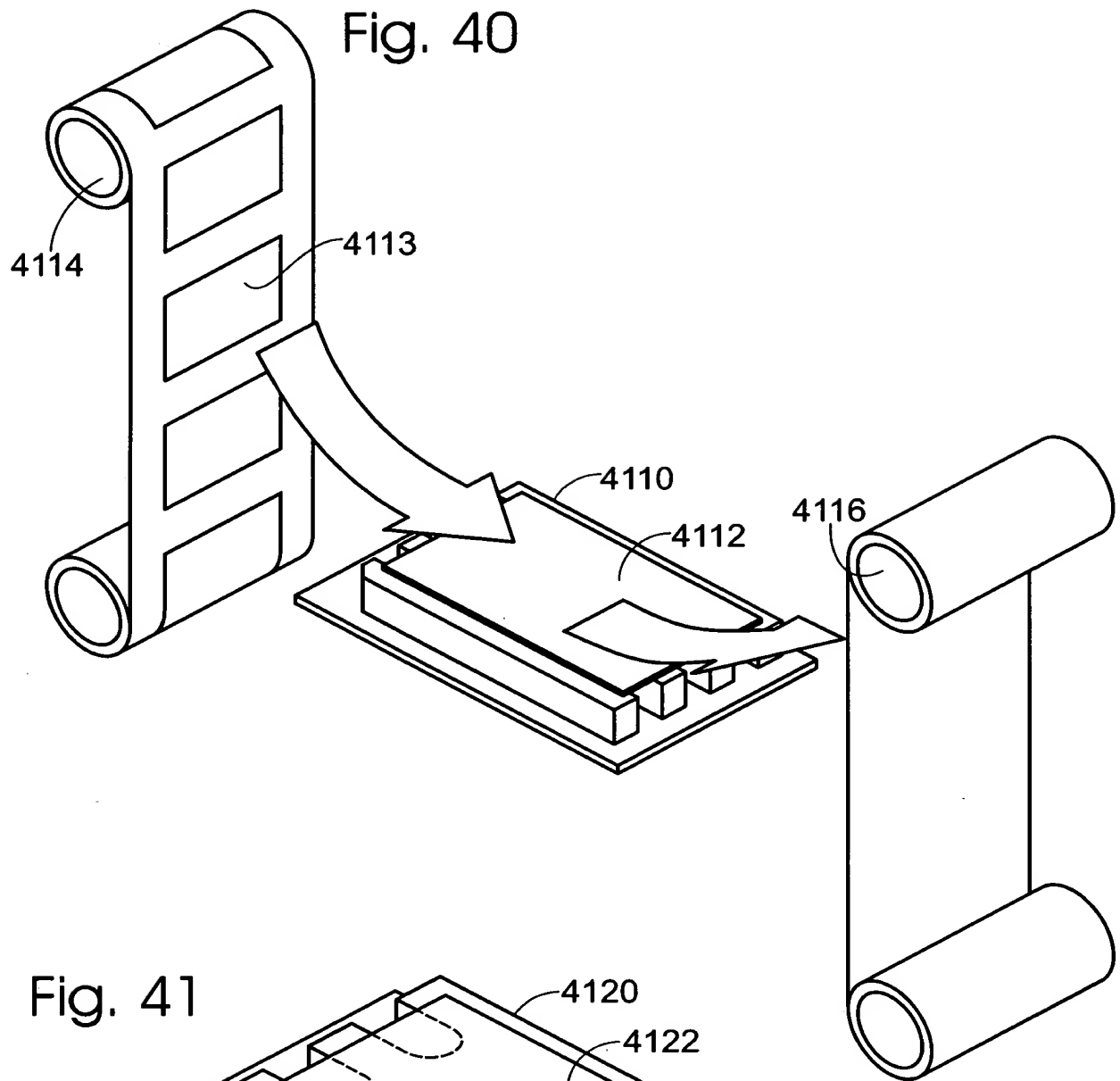


Fig. 41

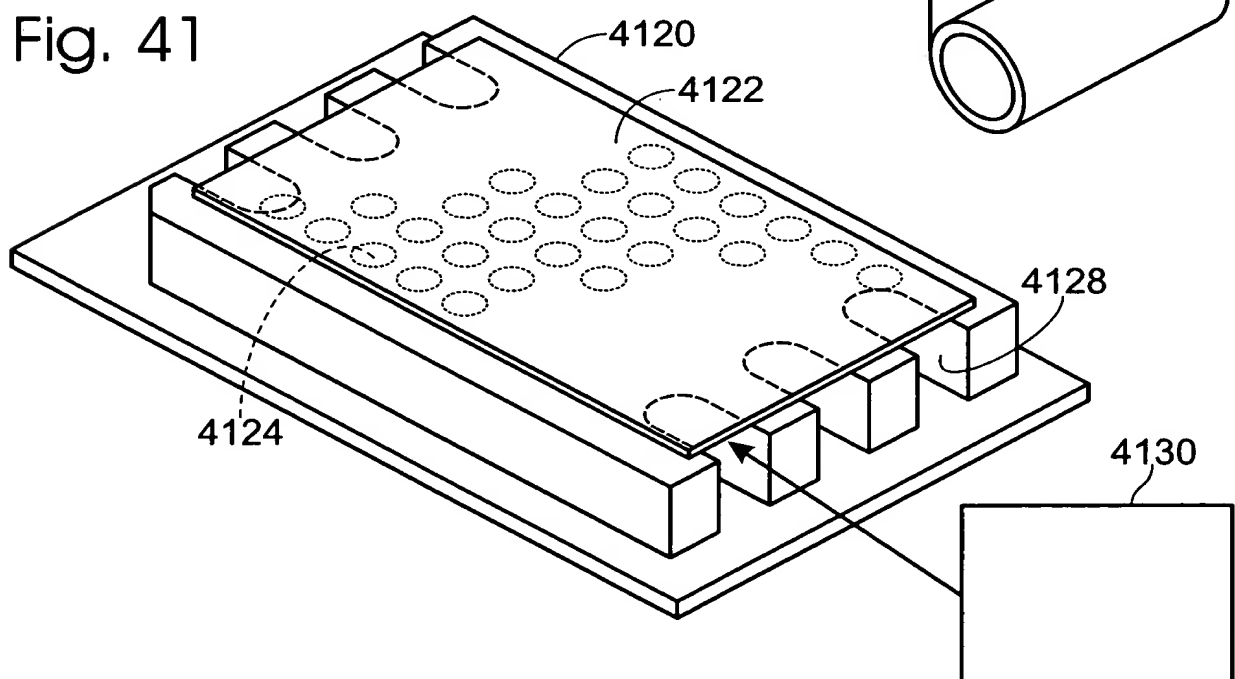


Fig. 42

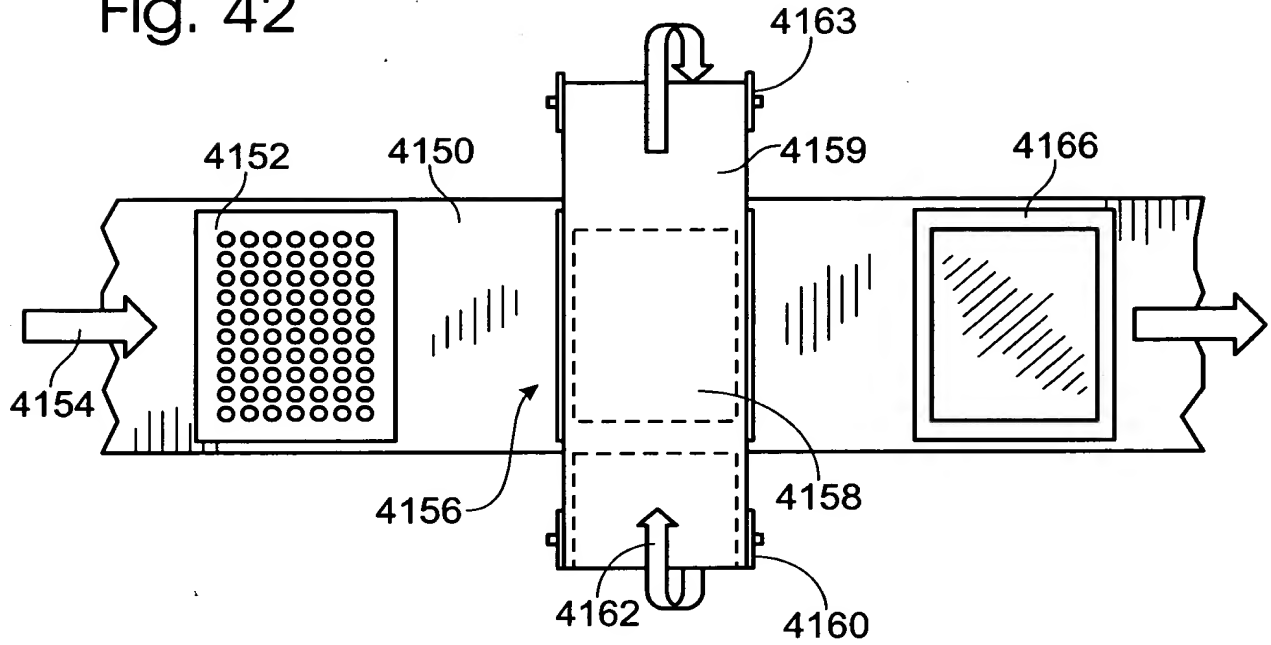


Fig. 43

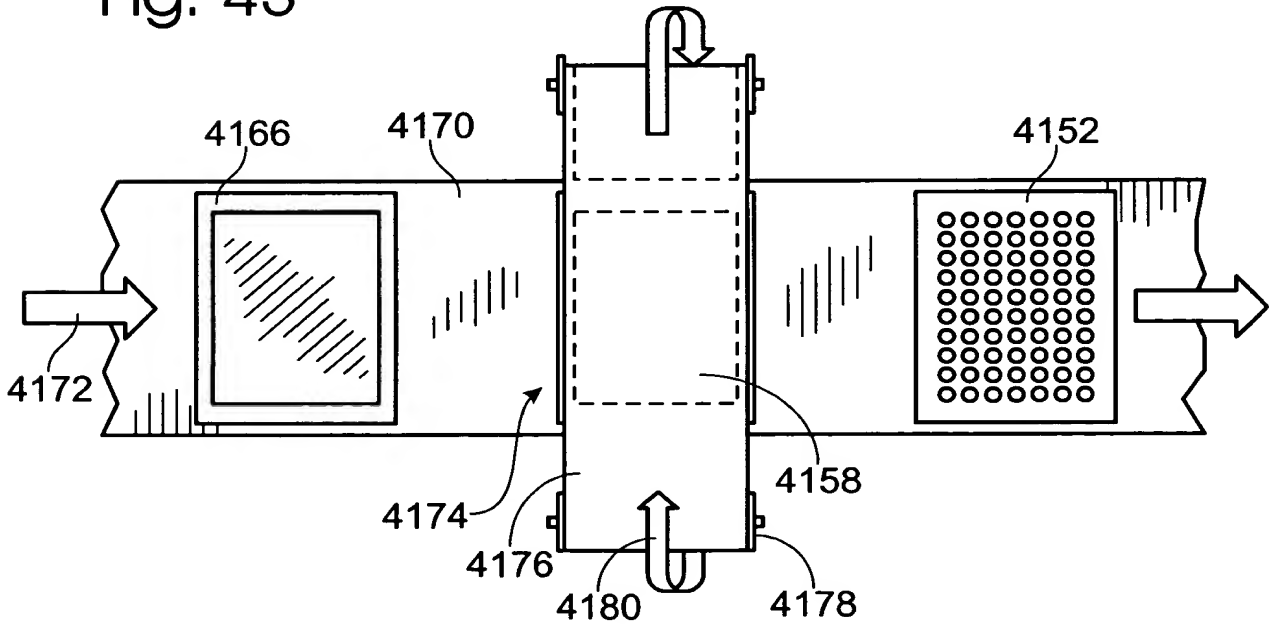


Fig. 44

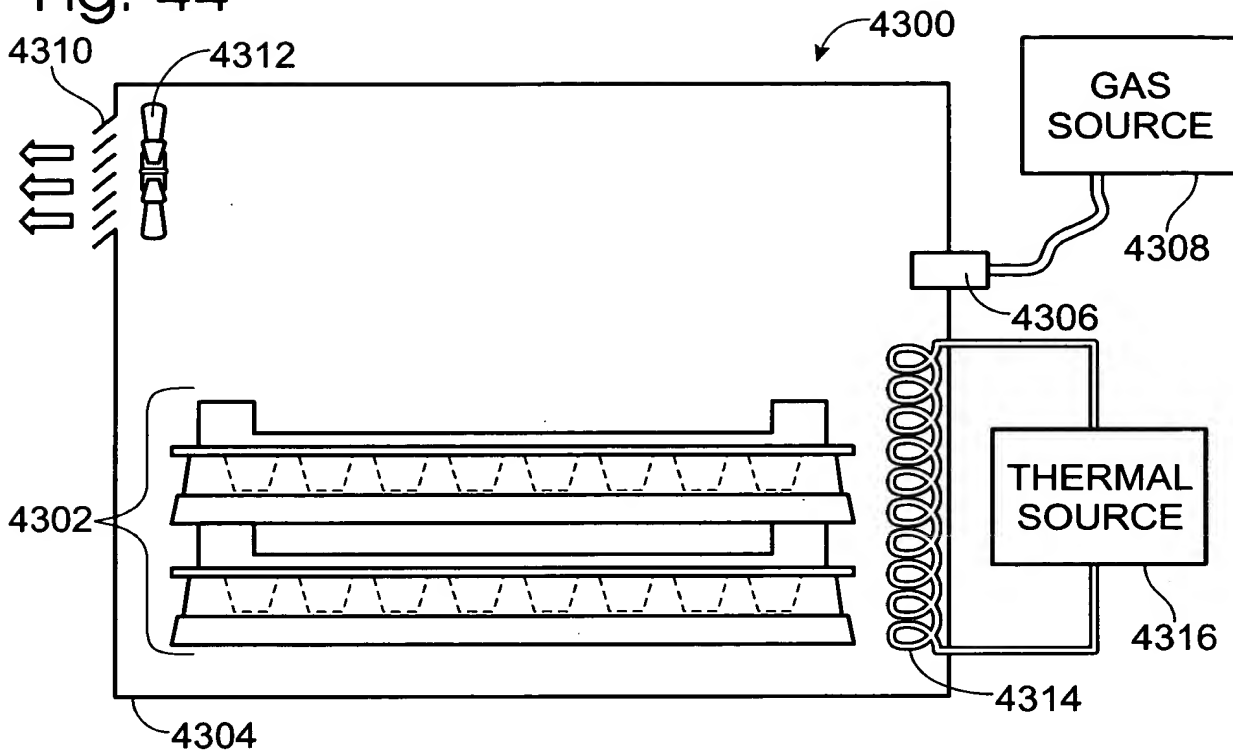


Fig. 45

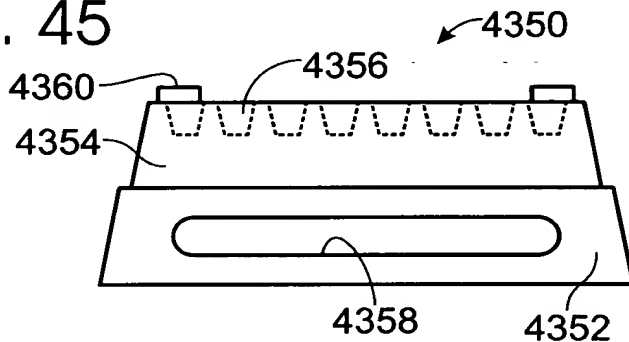


Fig. 46

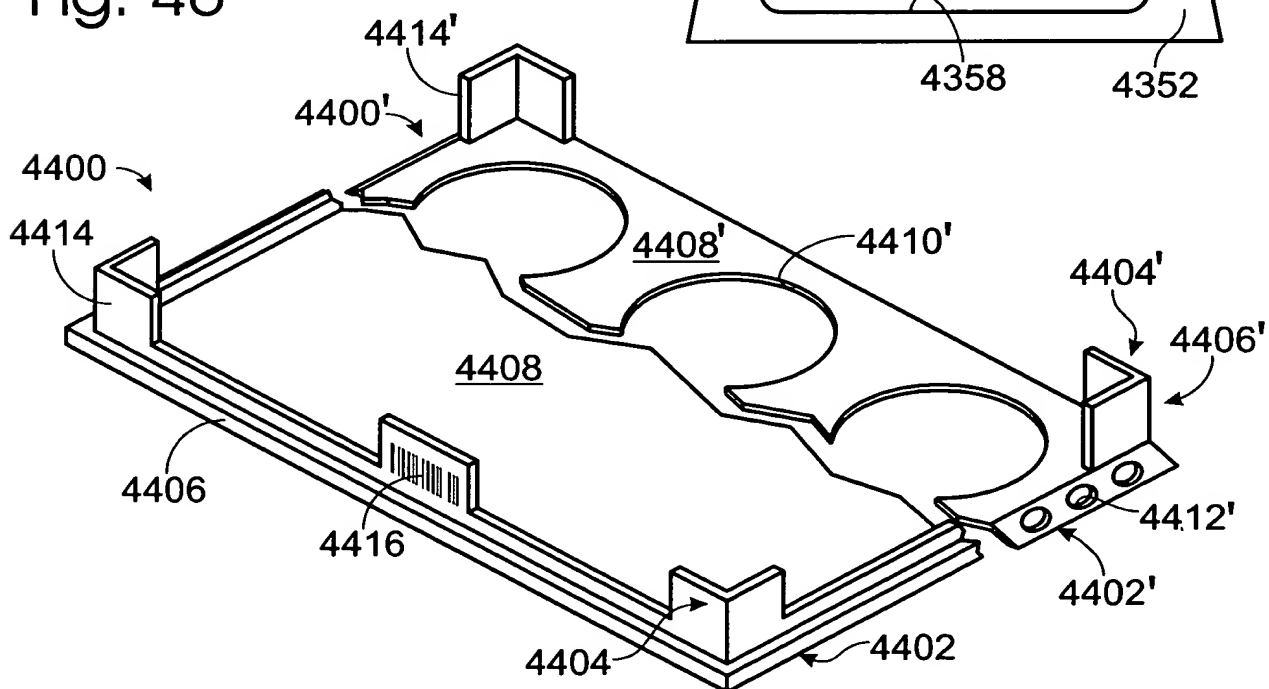




Fig. 47

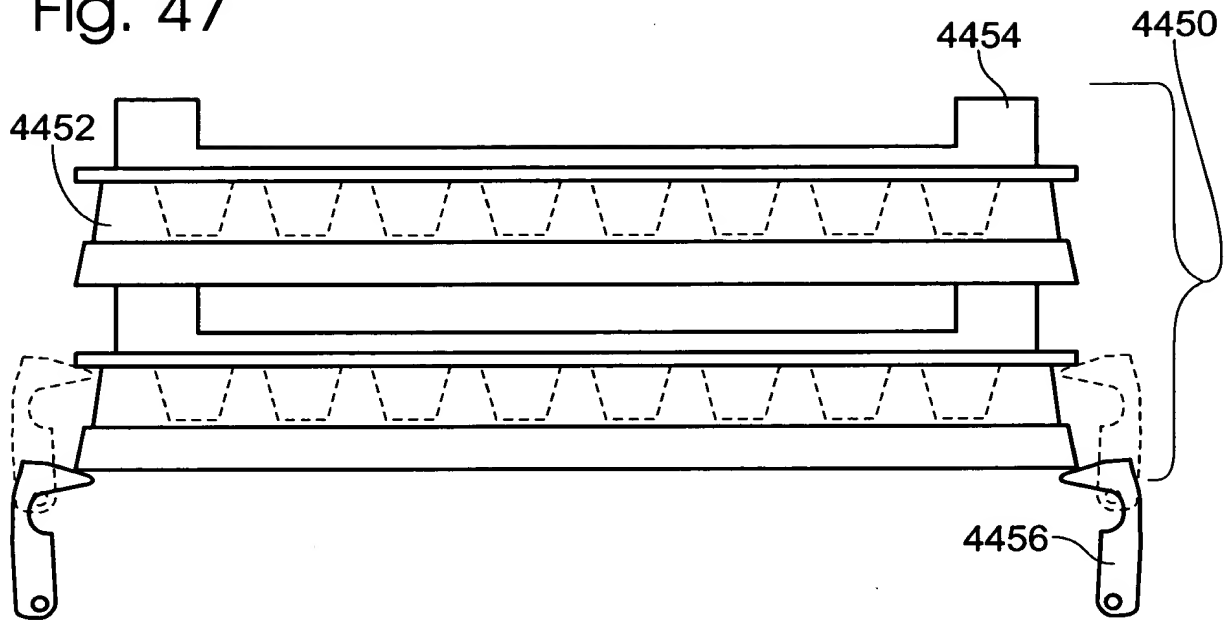
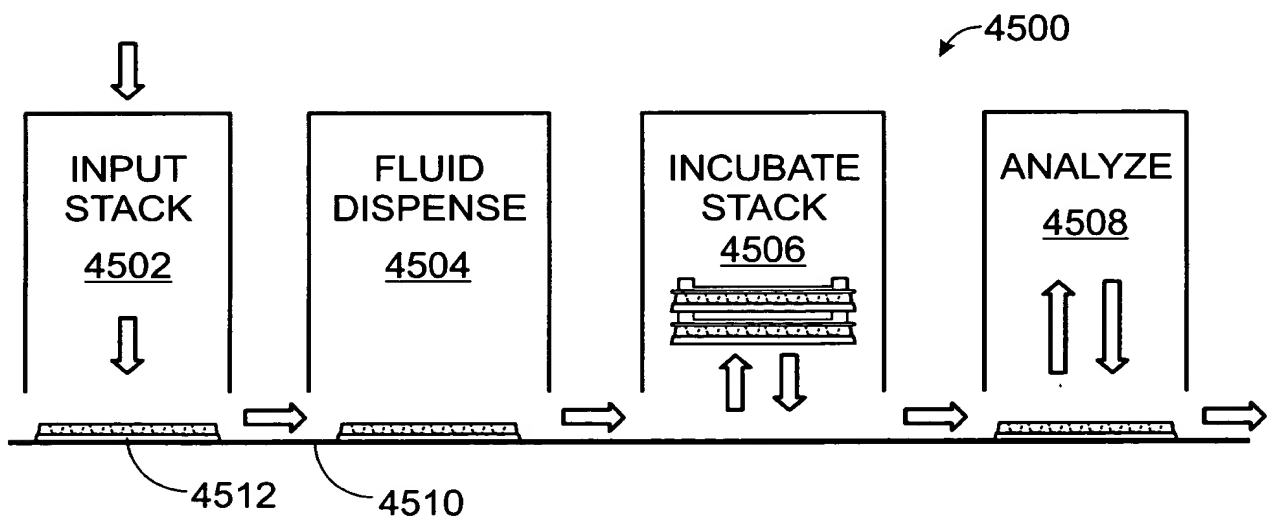


Fig. 48



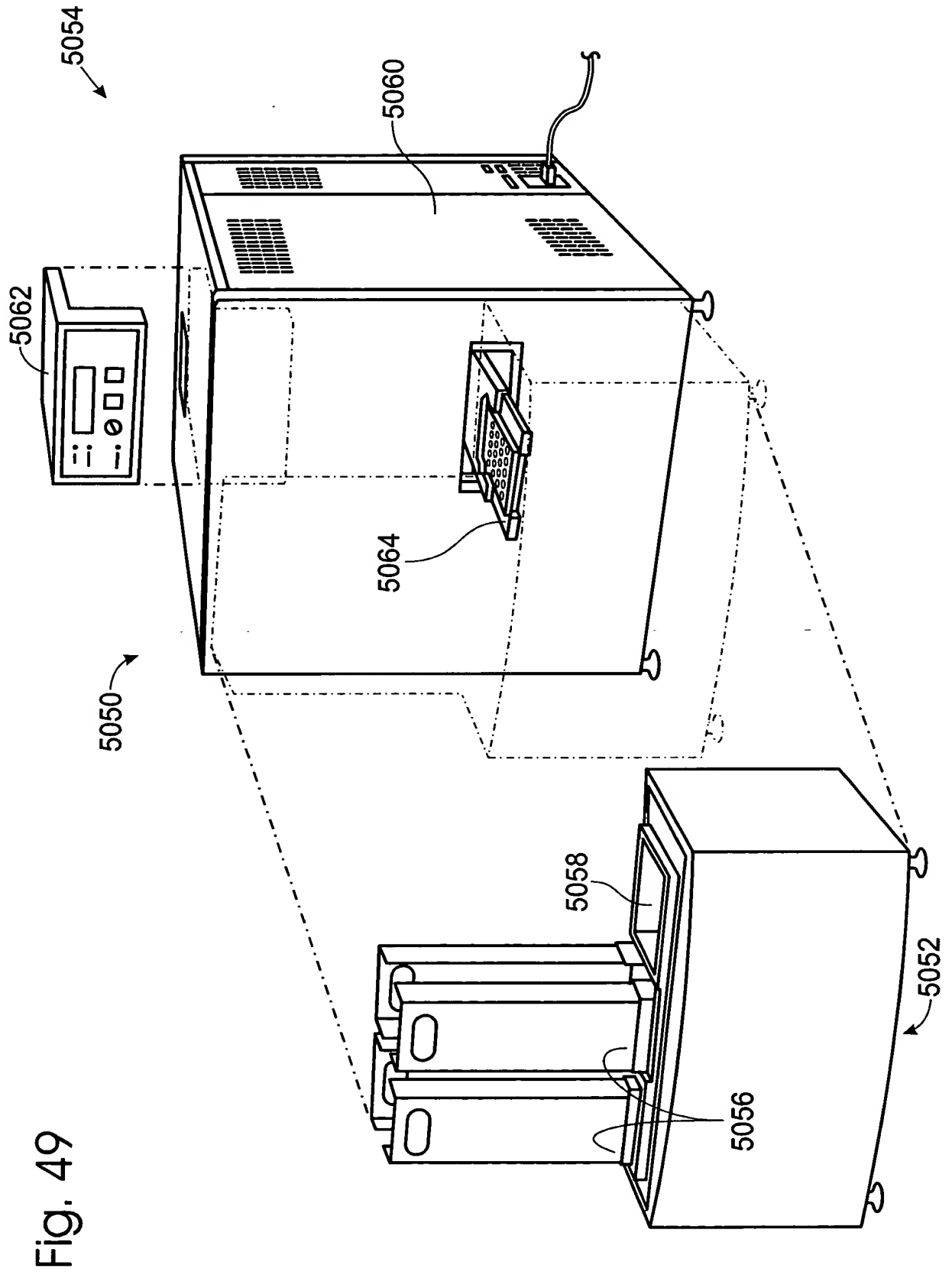


FIG. 49

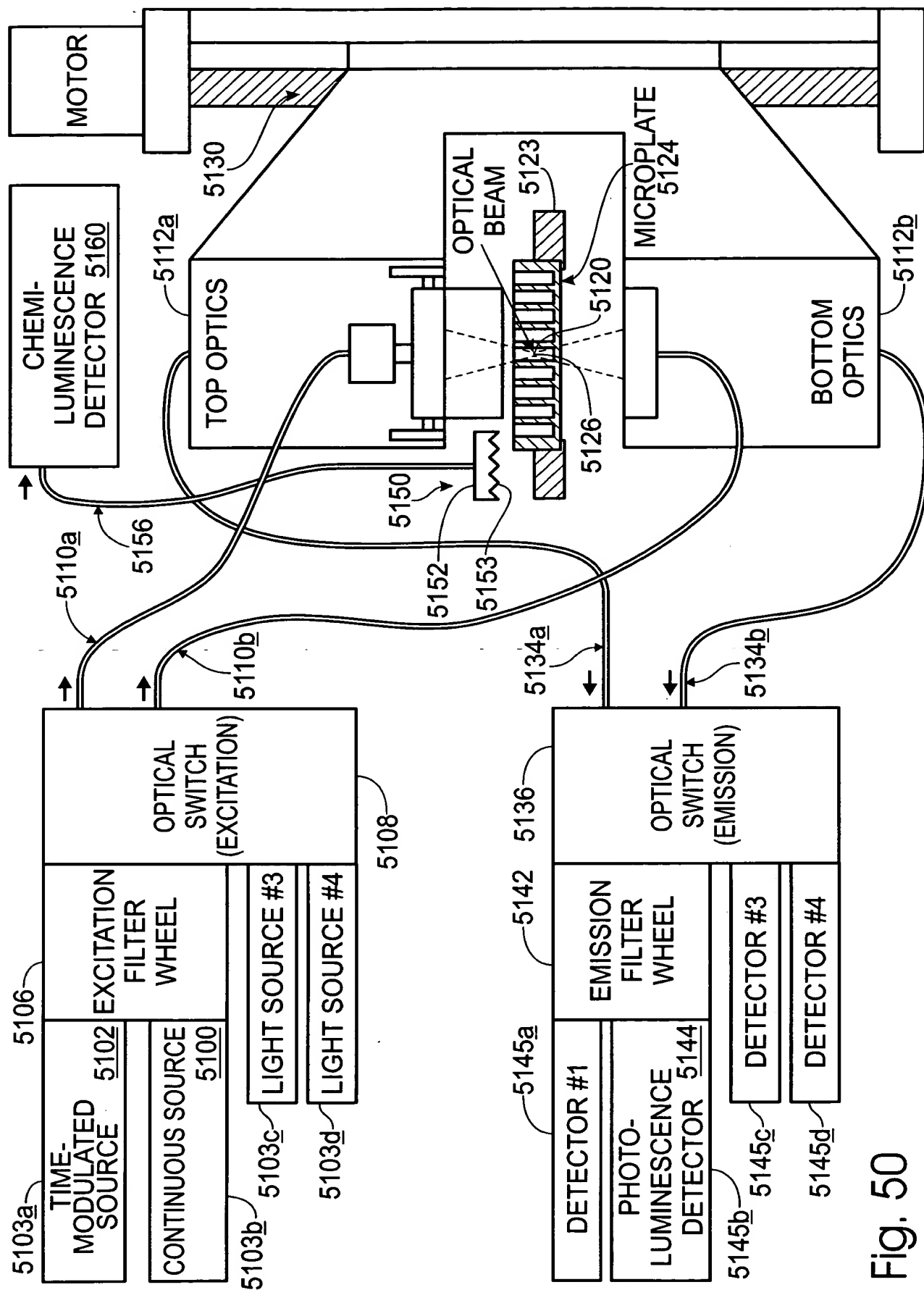


Fig. 50

Fig. 51

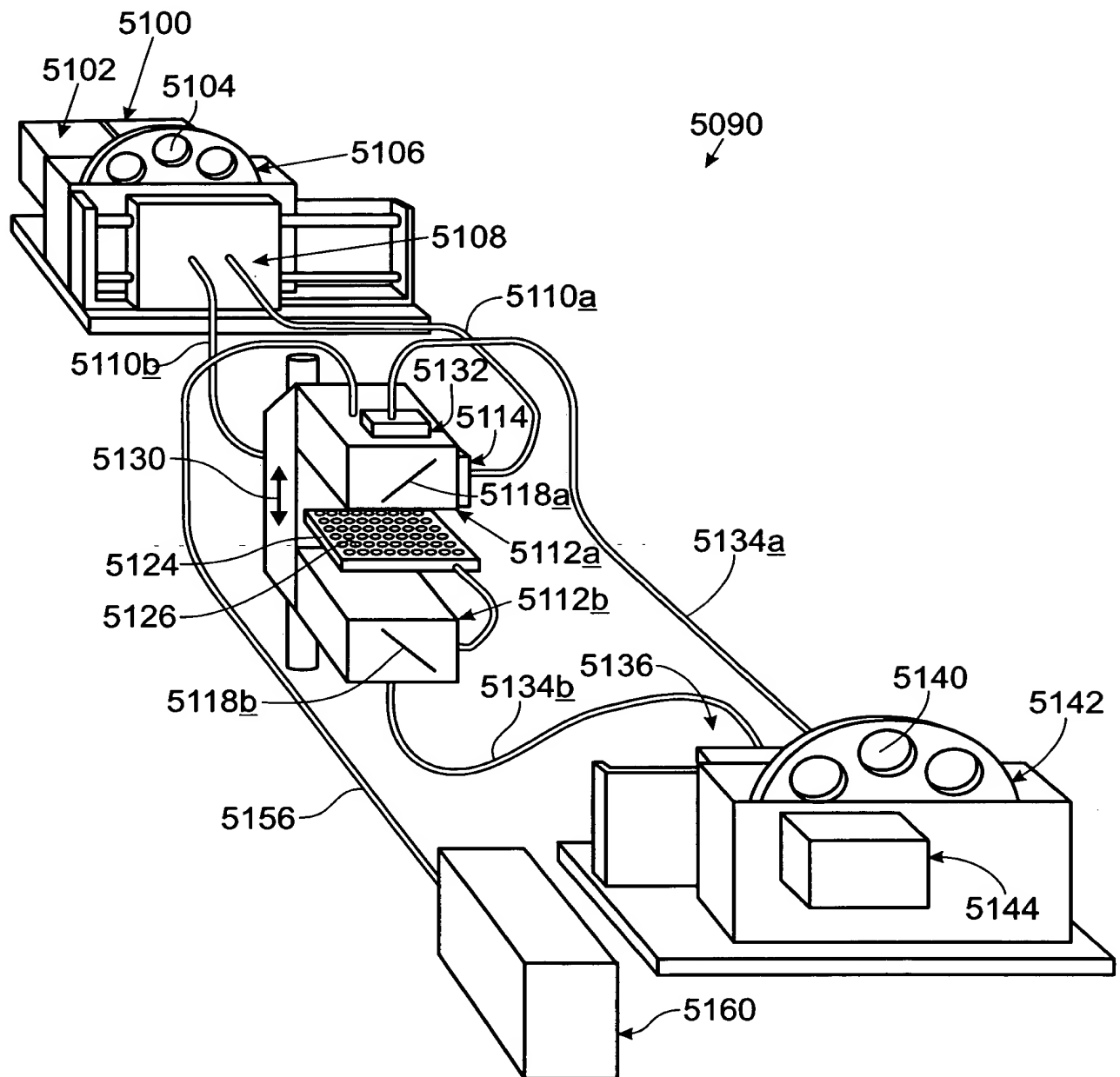


Fig. 52

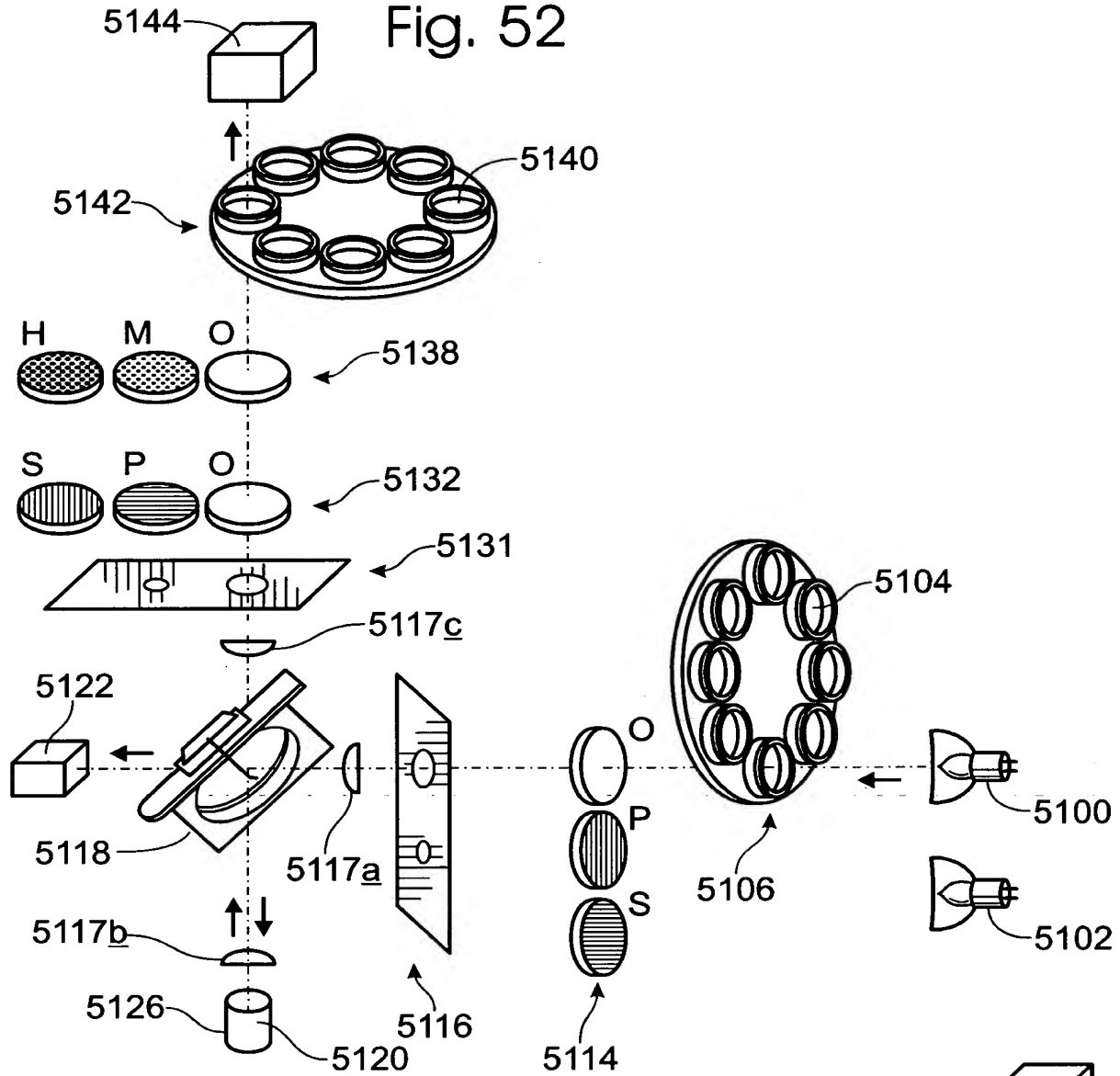


Fig. 53

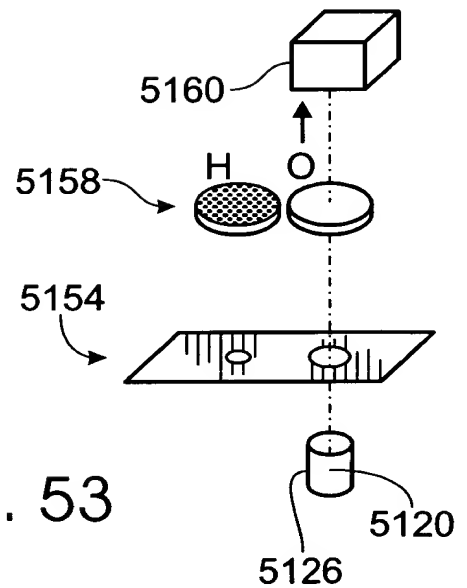


Fig. 54

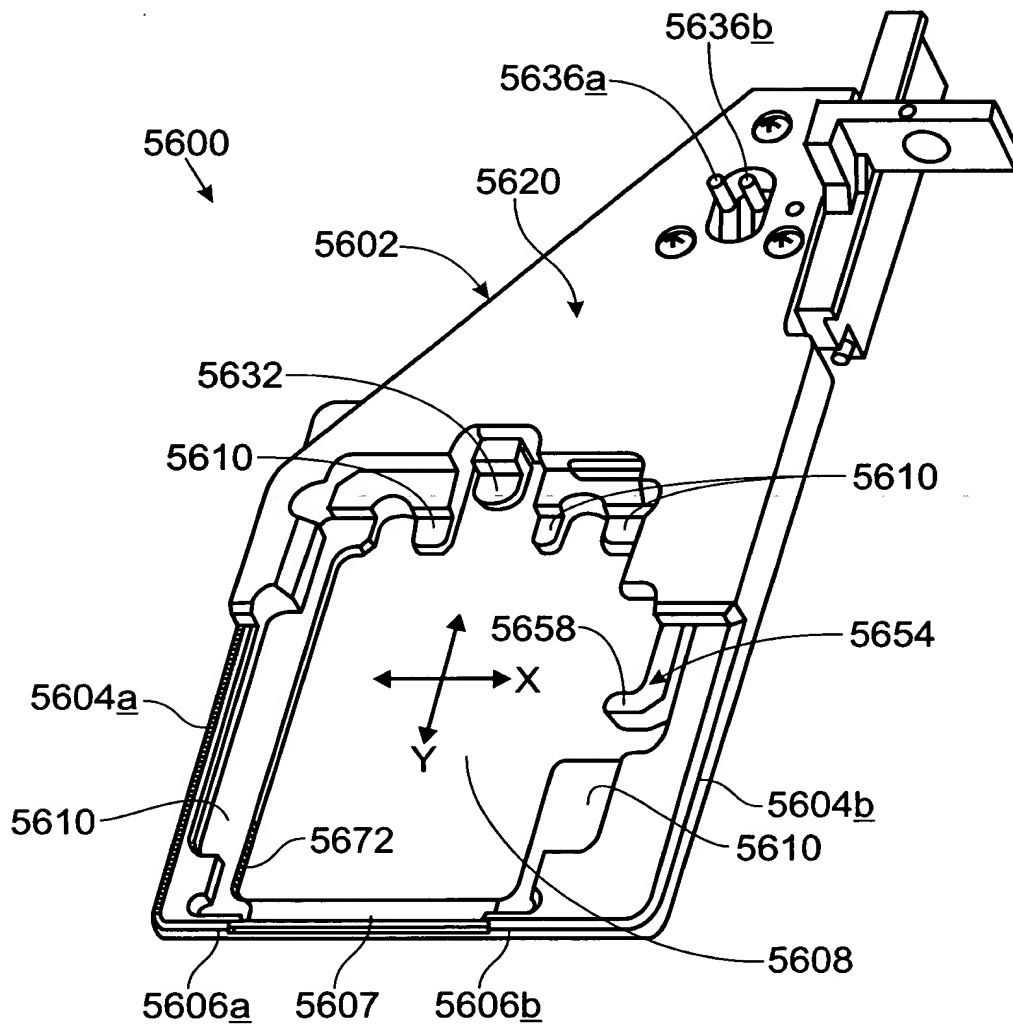


Fig. 55

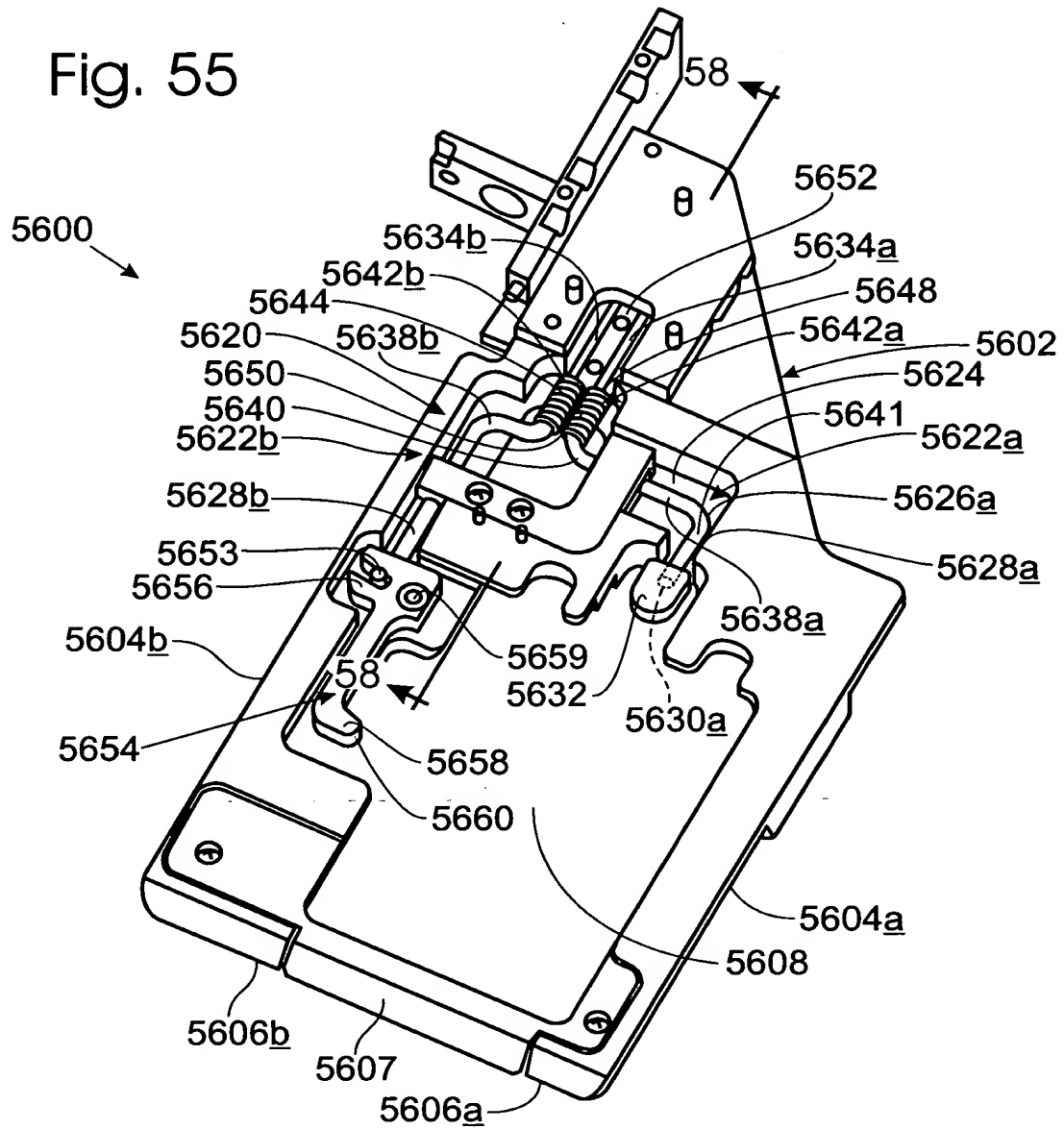


Fig. 56

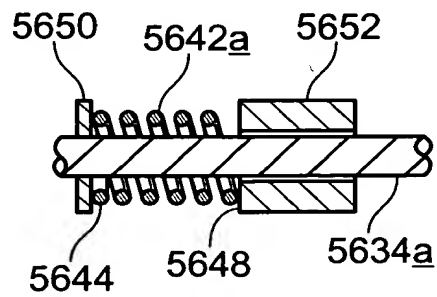


Fig. 57

